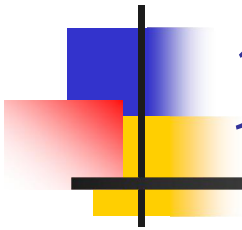
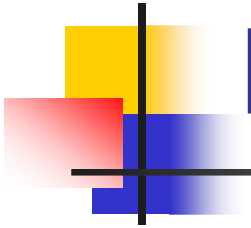


第七章 MOS存储器

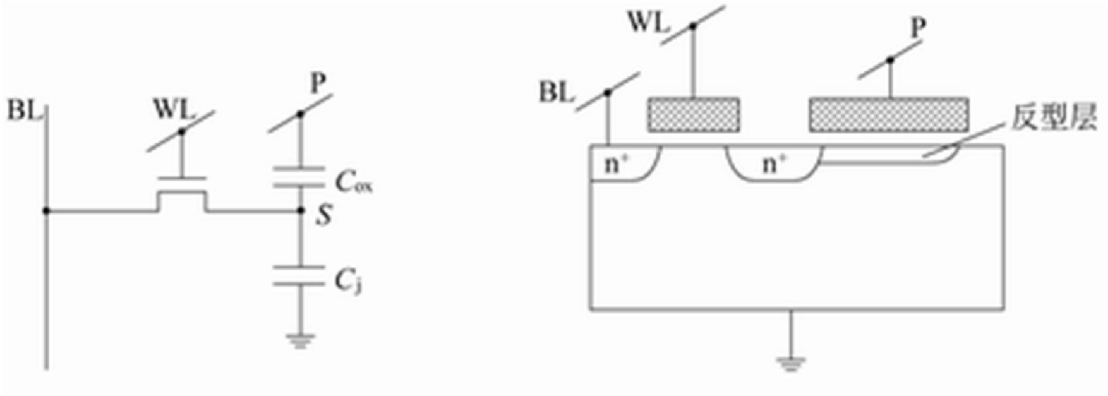
7.2 MOS存储器单元



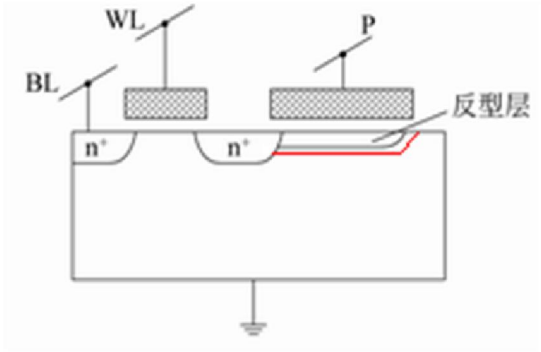
MOS存储器单元

- DRAM单元
- SRAM单元
- ROM单元

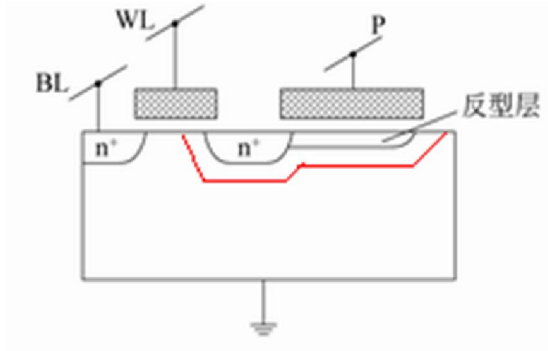
DRAM单元结构和工作原理



存储电容Cs=A(C_{ox}+C_j)

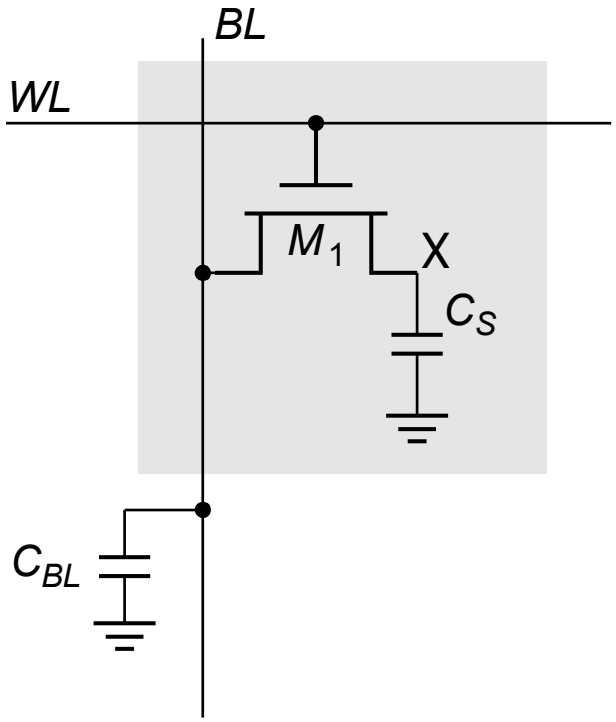


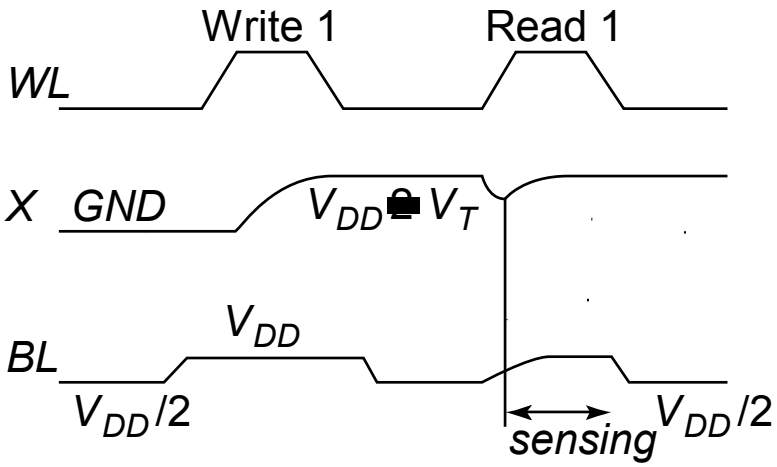
单元存“0”



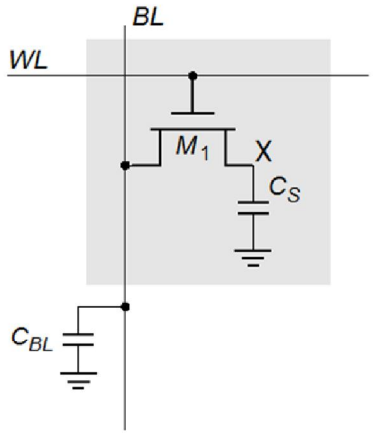
单元存”1”

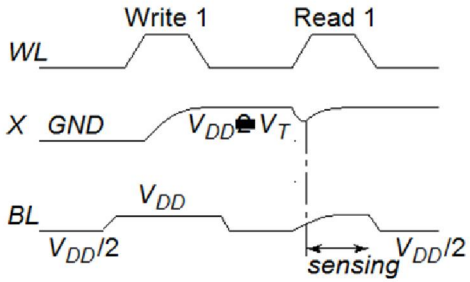
DRAM单元工作过程





信息的写入





■ 写“1”

预备动作：位线高电平

过程：字线高电平⟶门管导通⟶位线向存储电容充电

结果：存储节点的高电平：$V_{S1}=V_{DD}-V_{TN}$

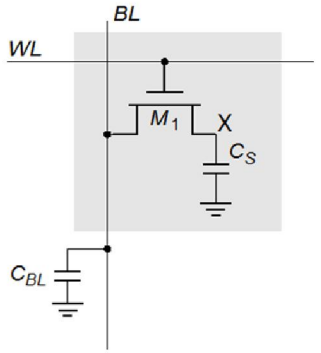
■ 写“0”

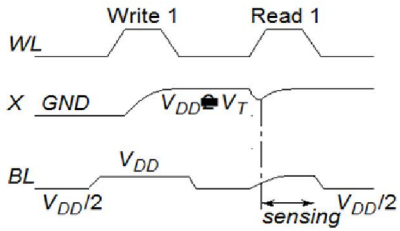
预备动作：位线低电平

过程：字线高电平⟶门管导通⟶位线对存储电容放电

结果：存储节点的低电平：$V_{S0}=0$

信息的读取





- 预备动作：位线预充电

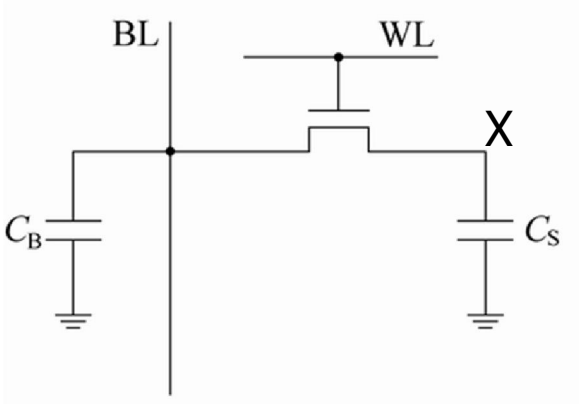
$$V_R = \frac{V_{S1} + V_{S0}}{2}$$

- 过程：字线高电平-〉门管导通-〉

存储电容和位线电容发生电荷分享

$$V_{BO} = \frac{V_R C_B + V_{SO} C_S}{C_B + C_S} < V_R$$

$$V_{B1} = \frac{V_R C_B + V_{S1} C_S}{C_B + C_S} > V_R$$



$$V_{BO} = \frac{V_R C_B + V_{SO} C_S}{C_B + C_S} < V_R$$

电荷传输效率

$$V_{B1} = \frac{V_R C_B + V_{S1} C_S}{C_B + C_S} > V_R$$

- 为了反映DRAM单元读出特性，引入单元电荷传输效率的参数T

$$T = \frac{\Delta V_B}{\Delta V_S} = \frac{V_{B1} - V_{B0}}{V_{S1} - V_{S0}} = \frac{1}{1 + C_B / C_S}$$

由于位线电容比存储电容大很多，因此电荷传输效率远小于1

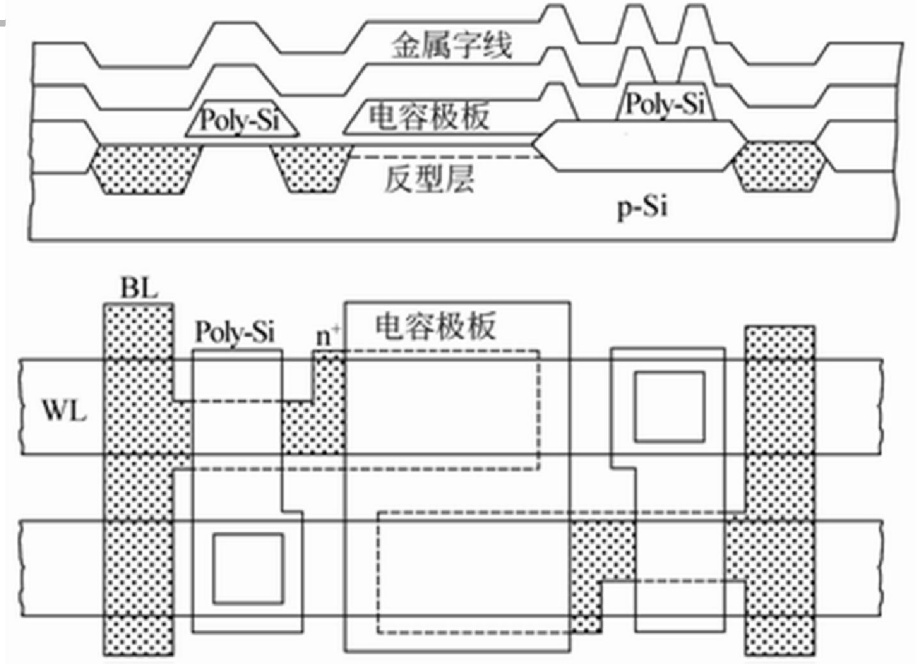
DRAM读操作存在**2**个问题: 读出后单元信号被破坏,
读出信号微弱

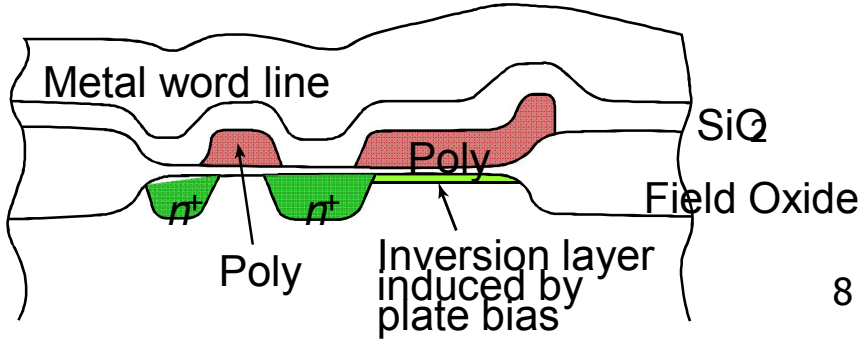
解决办法: 设置灵敏再生放大器**(S/R)**

DRAM单元结构

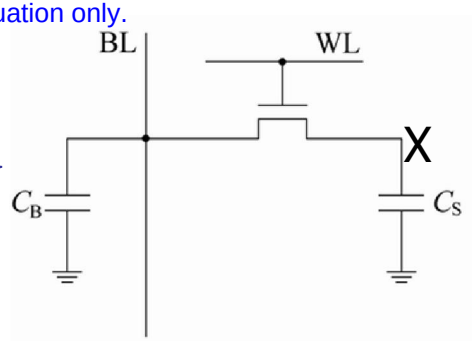
$$T=\frac{\Delta V_B}{\Delta V_S}=\frac{V_{B1}-V_{B0}}{V_{S1}-V_{S0}}=\frac{1}{1+C_B/C_S}$$

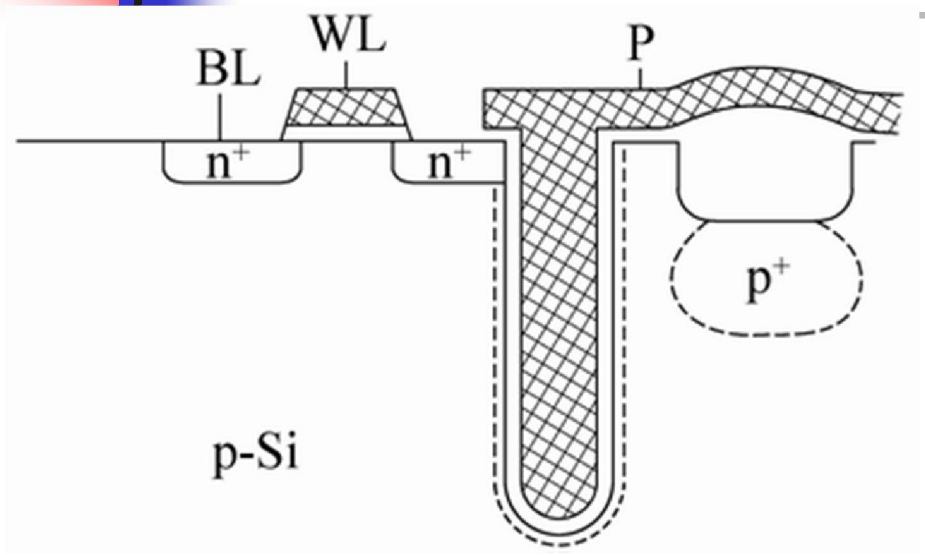
- 性能优值：增加存储单元电容值
- 面积优值：减小单元占用面积
- 利用立体结构在不增加平面面积情况下，增加存储电容
- 利用高**K**材料增加存储电容

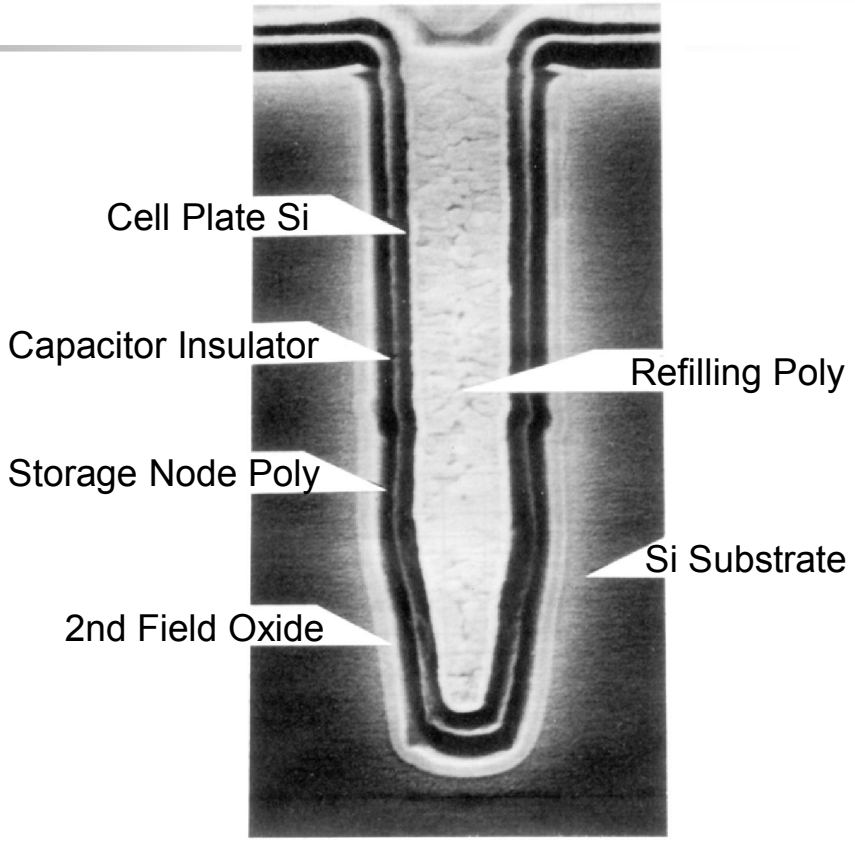




DRAM单元结构：沟槽电容



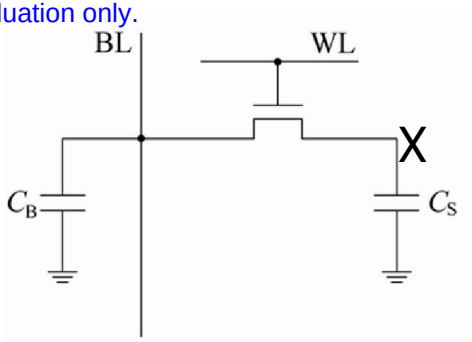


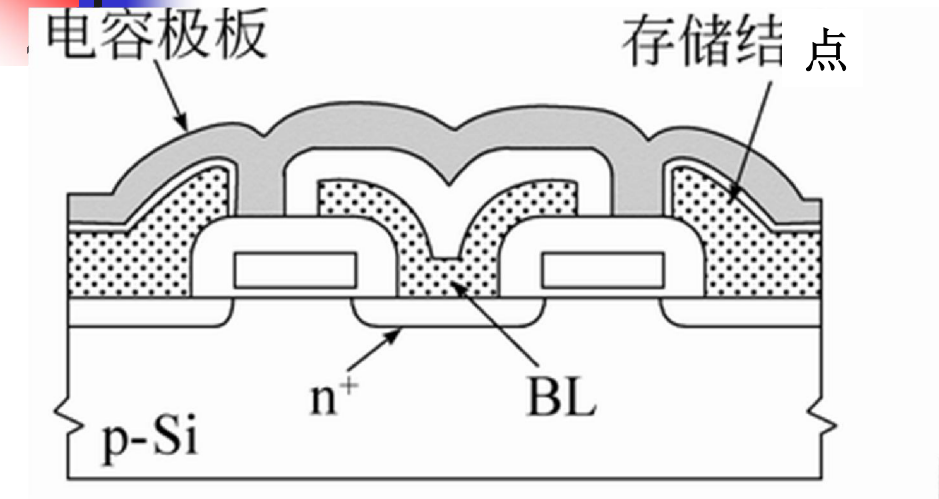


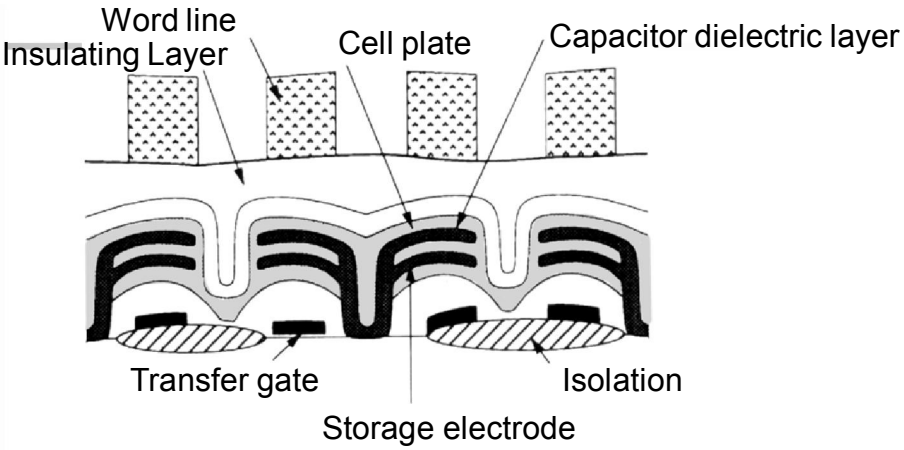
- 垂直方向，向下拓展空间

Trench Cell

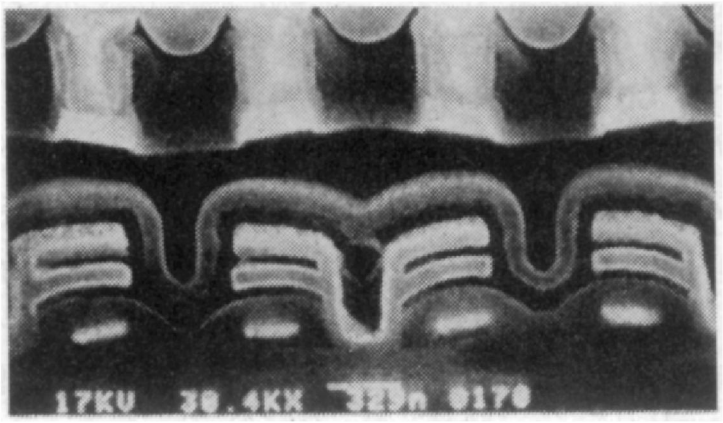
DRAM单元结构：叠置电容





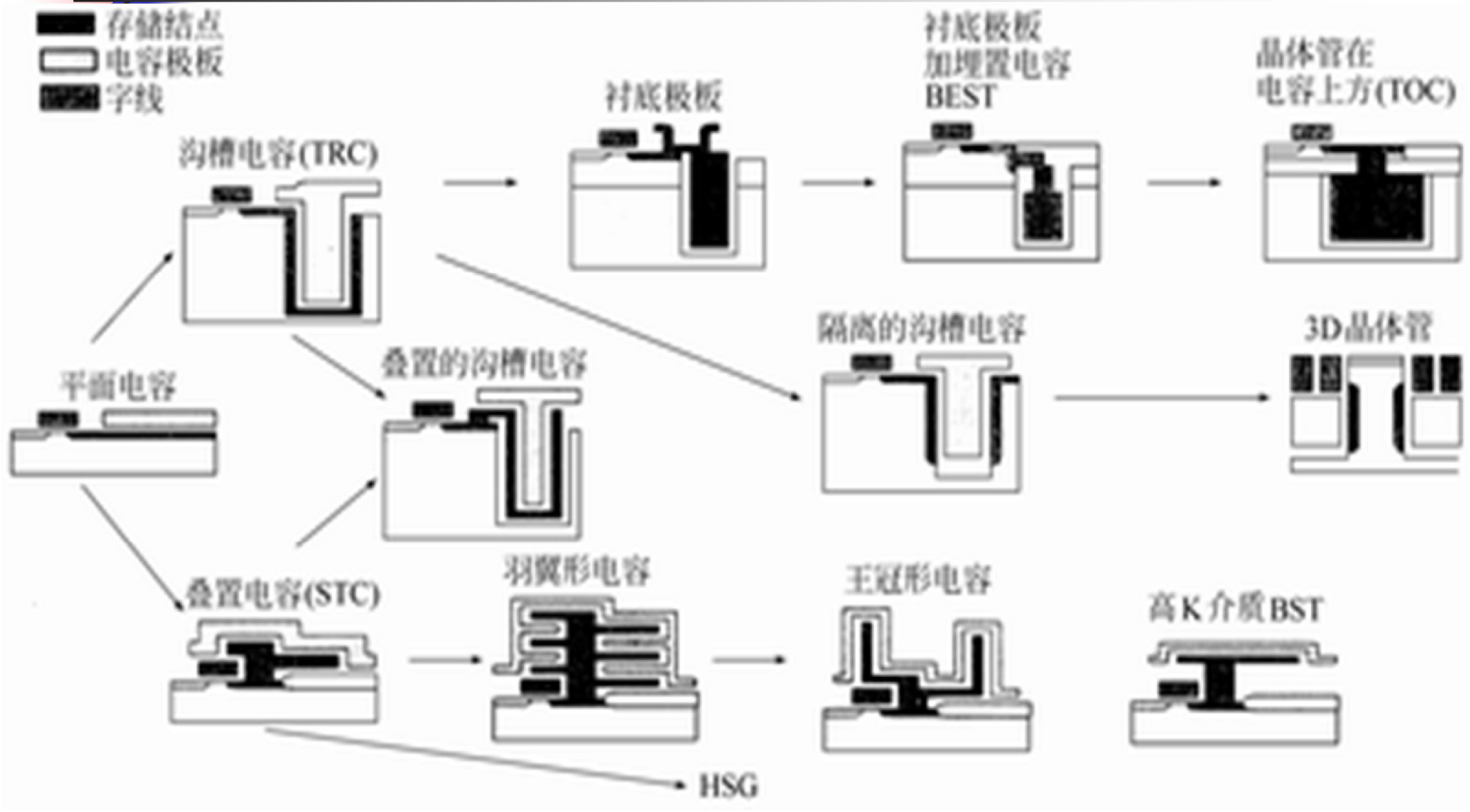


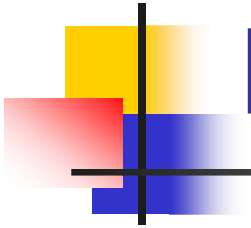
- 垂直方向：向上拓展空间



Stacked-capacitor Cell

DRAM单元结构发展



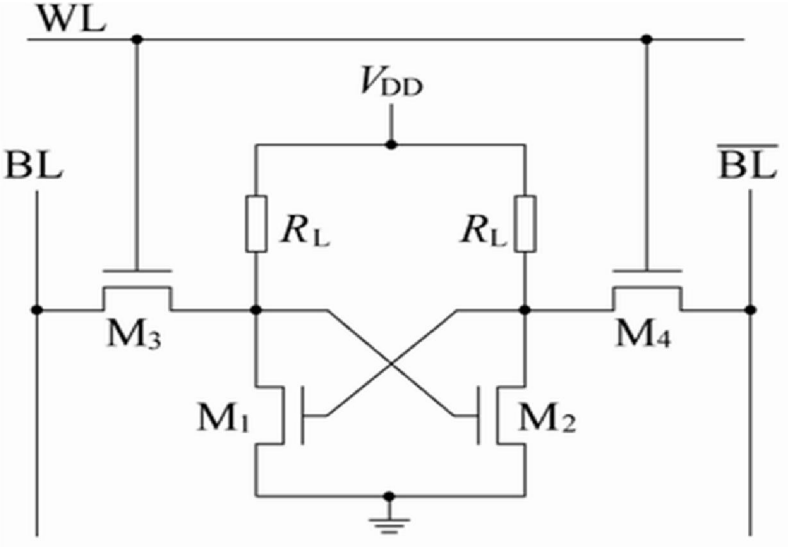


MOS存储器单元

- DRAM单元
- SRAM单元
- ROM单元

SRAM单元结构和工作原理

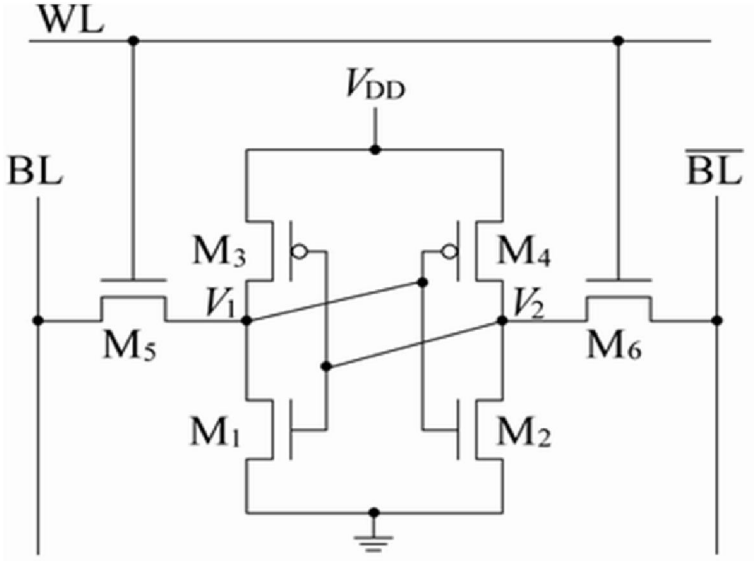
- 高阻多晶硅电阻负载的单元



问题：功耗与可靠性的矛盾

13

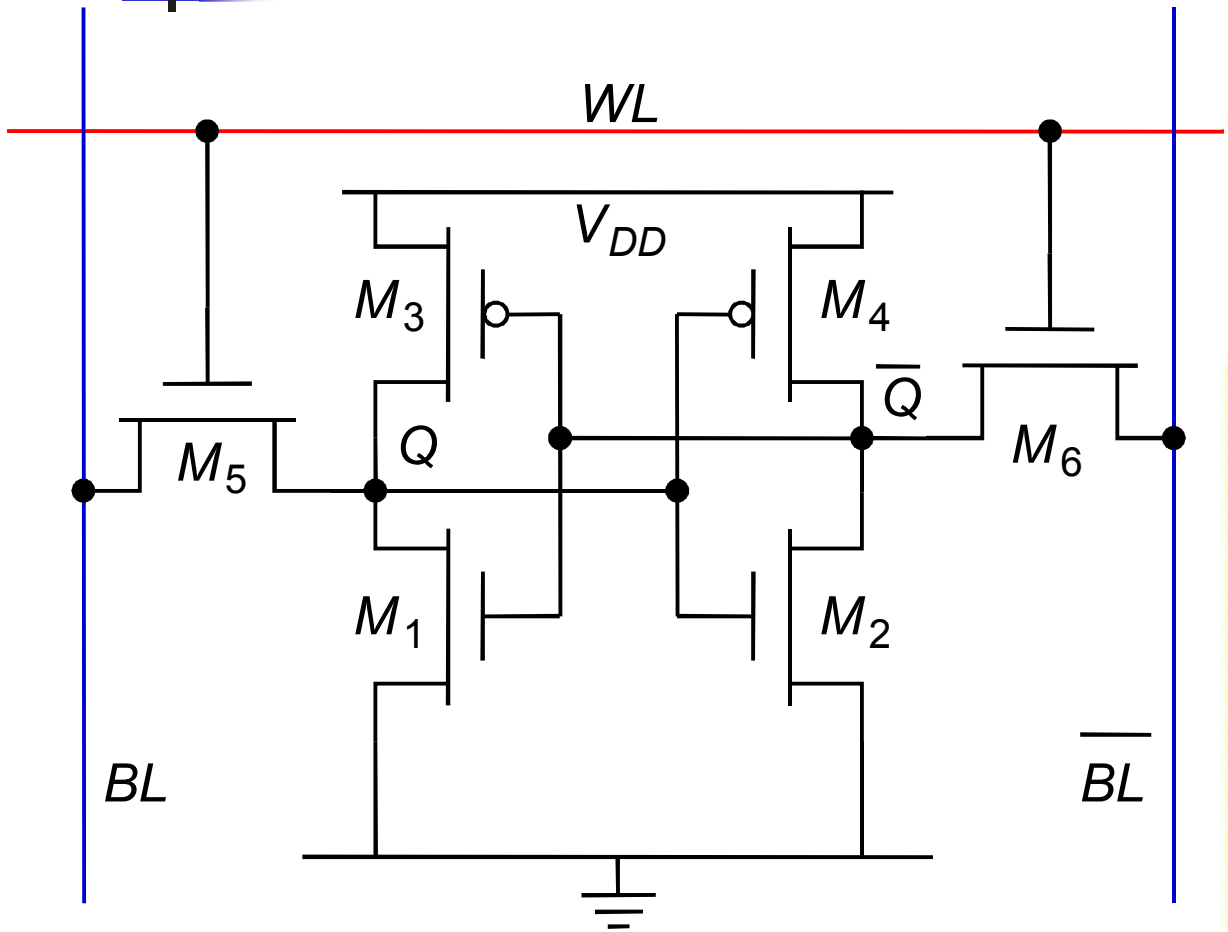
CMOS单元电路

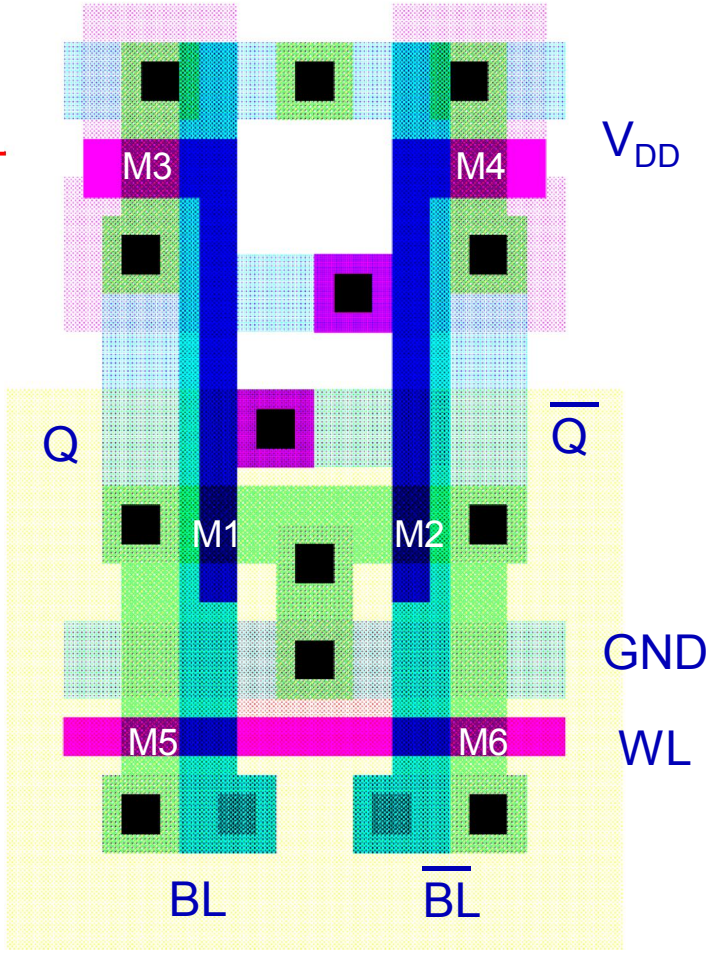


- 解决电阻负载单元中功耗和可靠性的矛盾
- 优势：
  - 只有泄漏电流引起的静态功耗
  - 保证单元存储信息可靠

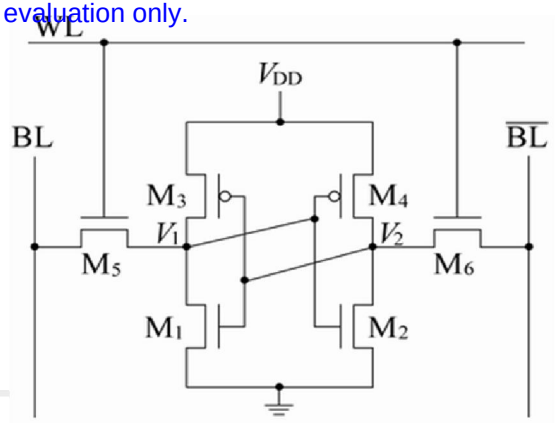
14

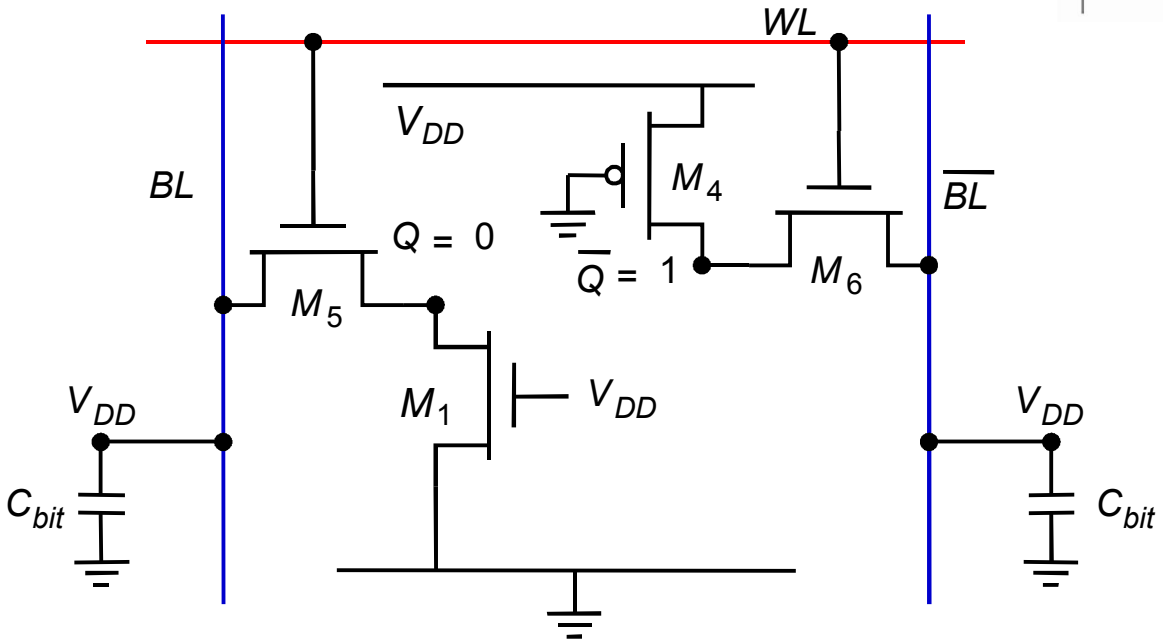
6-transistor CMOS SRAM Cell



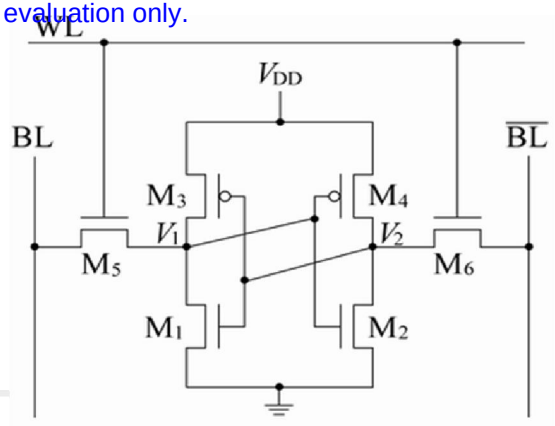


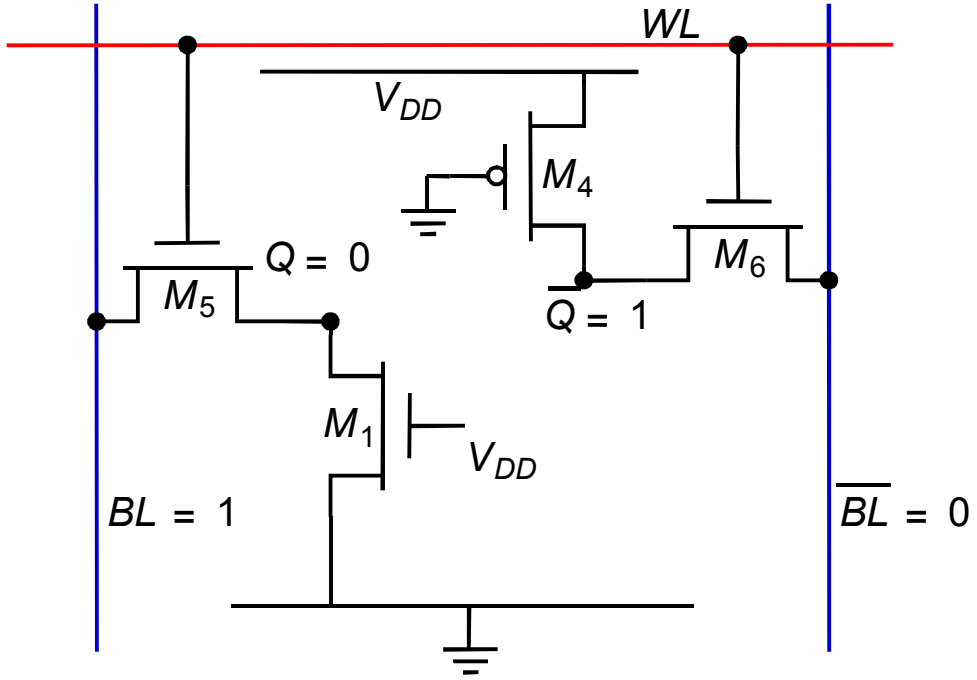
CMOS SRAM 读操作



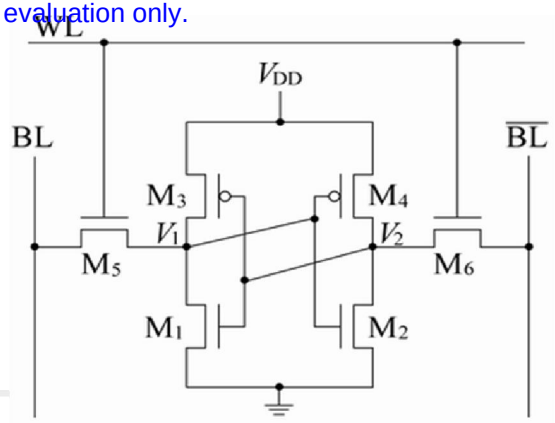


CMOS SRAM 写操作

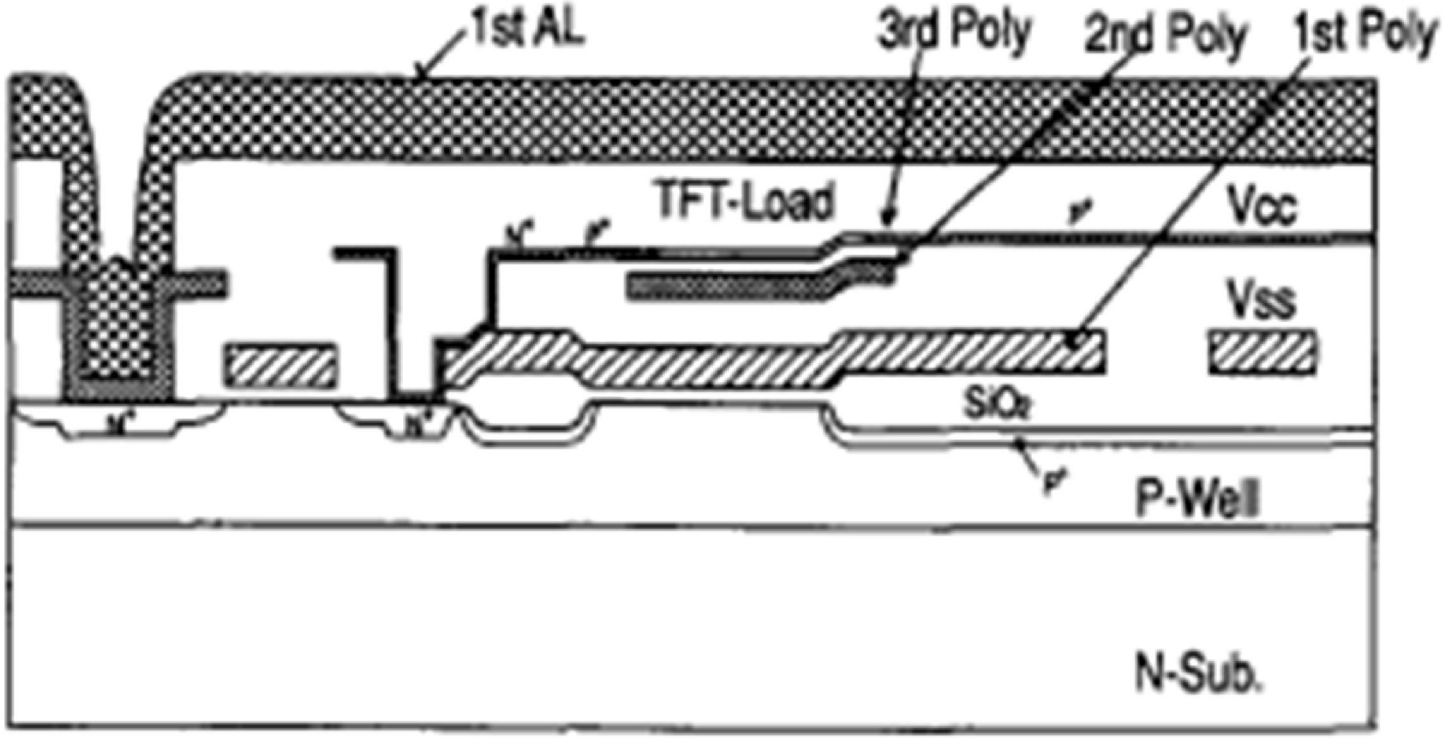




CMOS单元结构



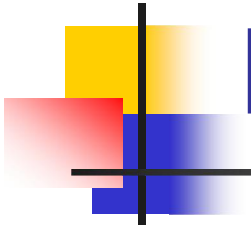
- TFT负载的CMOS单元



SRAM Characteristics

Table 12-2 Comparison of CMOS SRAM cells used in 1-Mbit memory (from [Takada91])

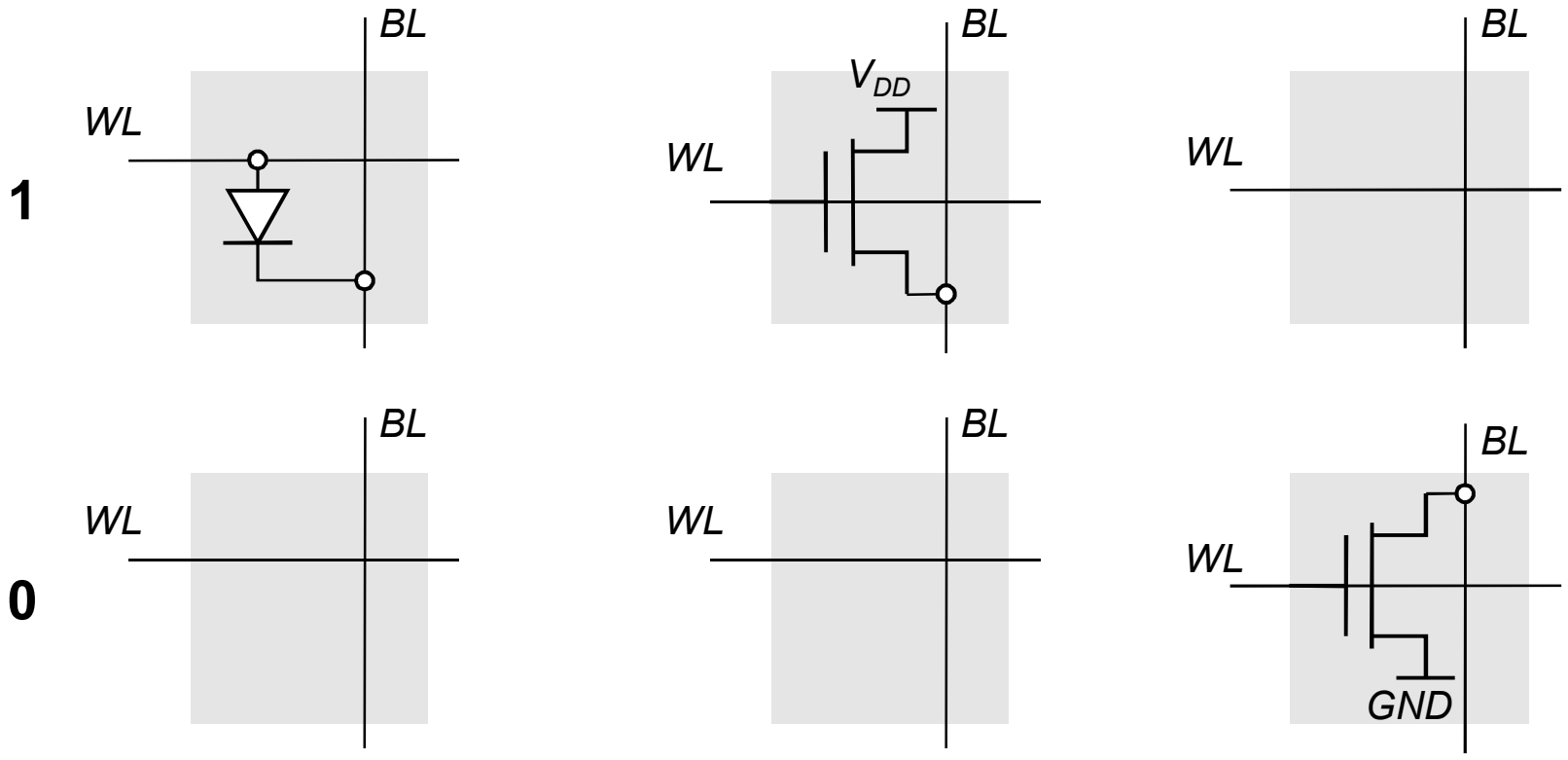
	Complementary CMOS	Resistive Load	TFT Cell
Number of transistors	6	4	4 (+2 TFT)
Cell size	58.2 μm^2 (0.7-µm rule)	40.8 μm^2 (0.7-µm rule)	41.1 μm^2 (0.8-µm rule)
Standby current (per cell)	10^{-15} A	10^{-12} A	10^{-13} A



MOS存储器单元

- DRAM单元
- SRAM单元
- ROM单元

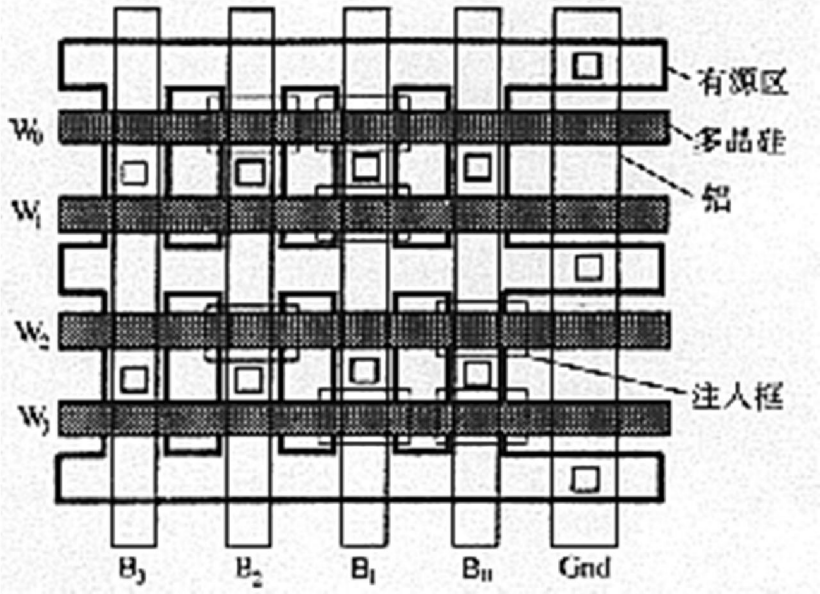
Read-Only Memory Cells

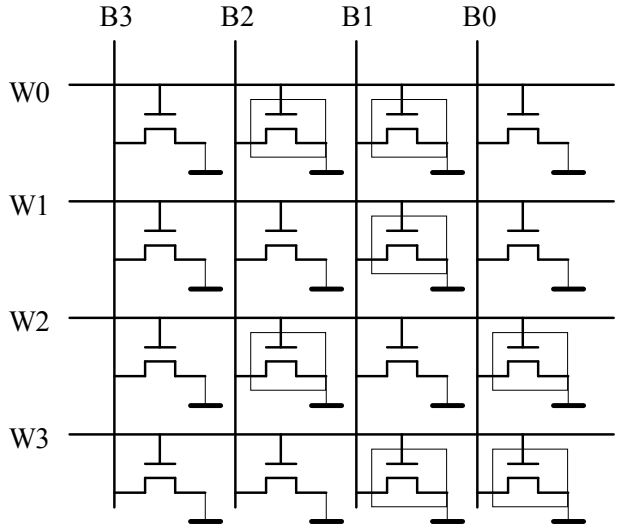


Diode ROM **MOS ROM 1** **MOS ROM 2**

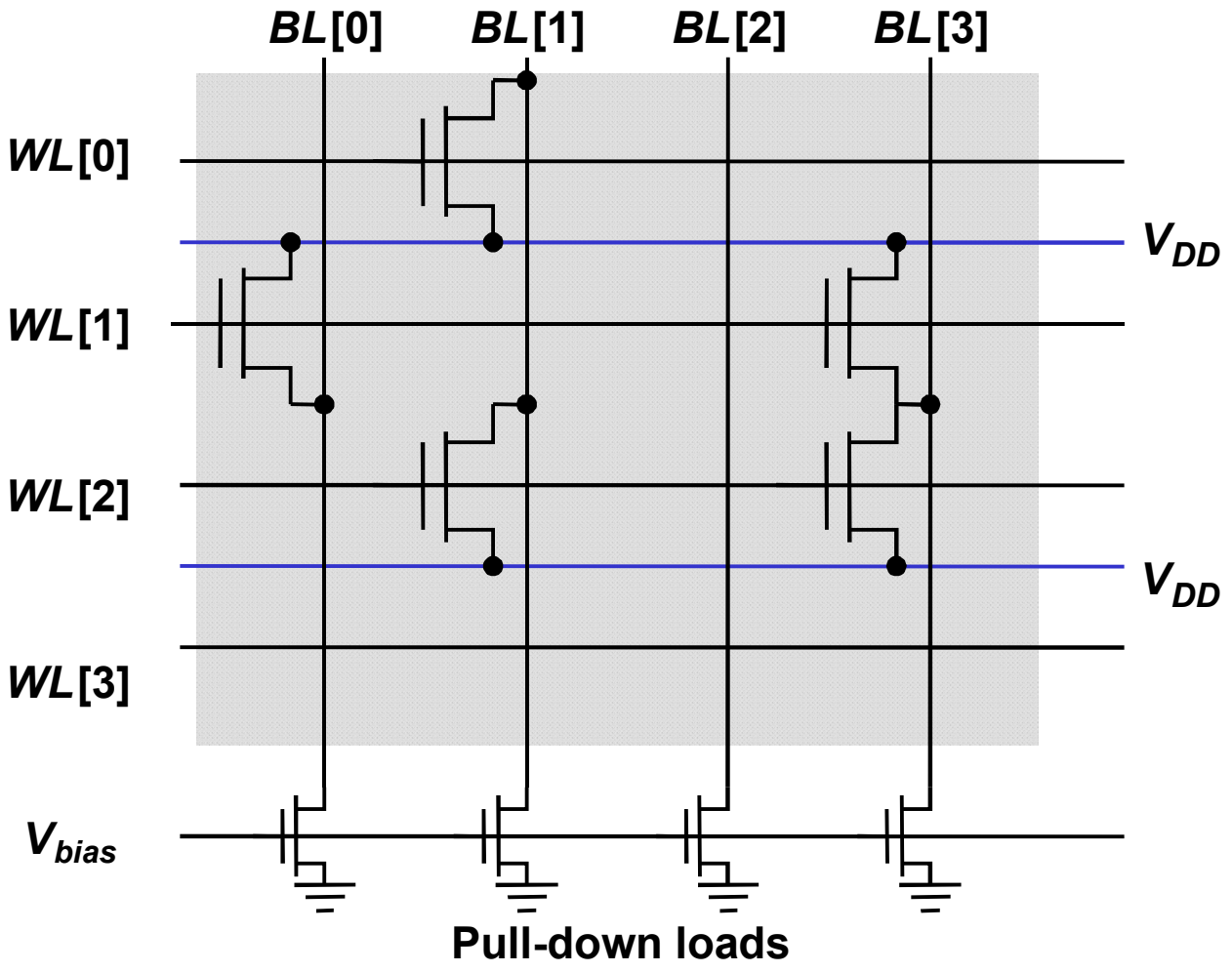
掩模编程的ROM单元

- 一个**MOS**管构成一个单元
- 用制作**MOS**管的某一次光刻版实现编程：
  - 离子输入，有源区，引线孔

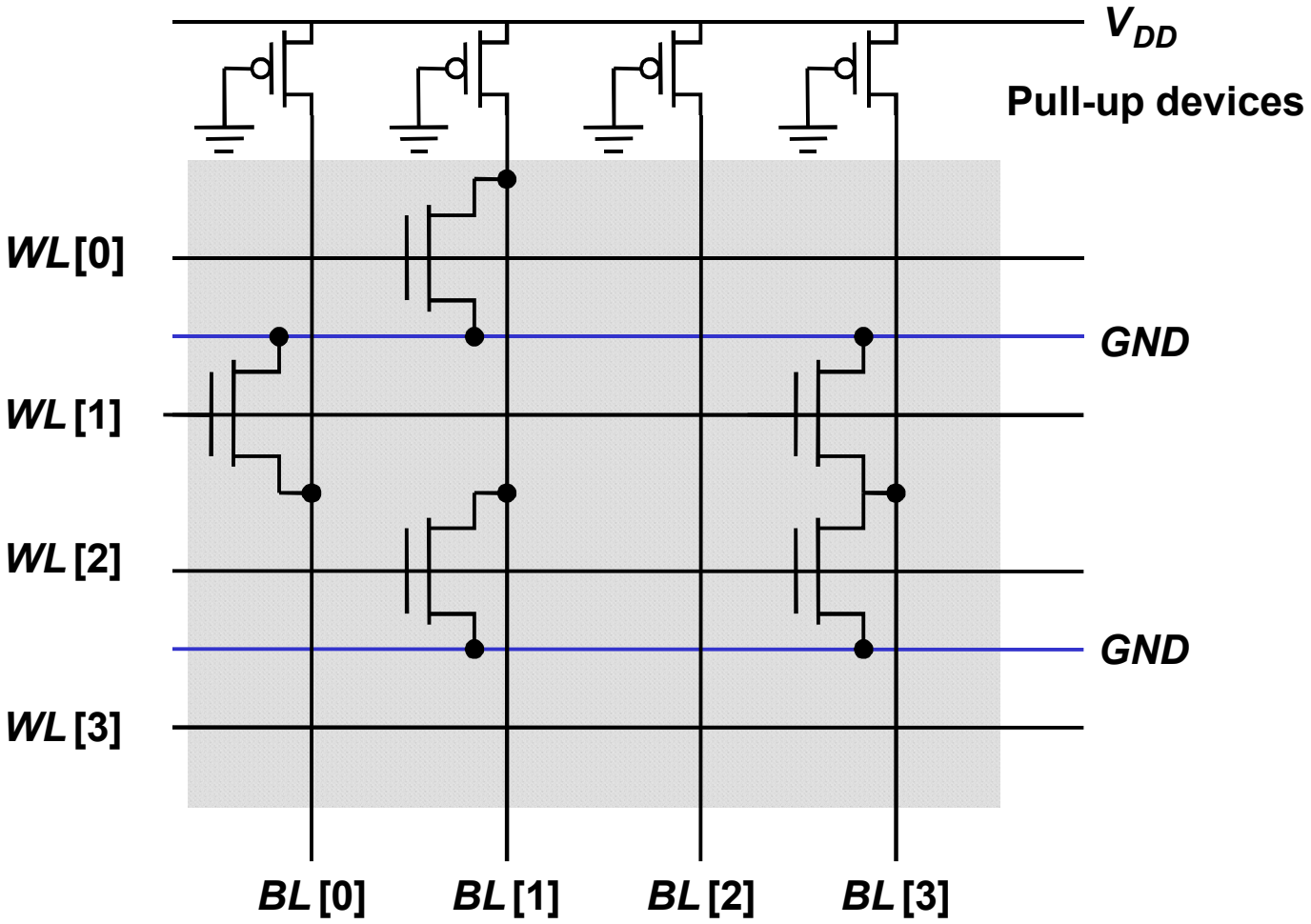




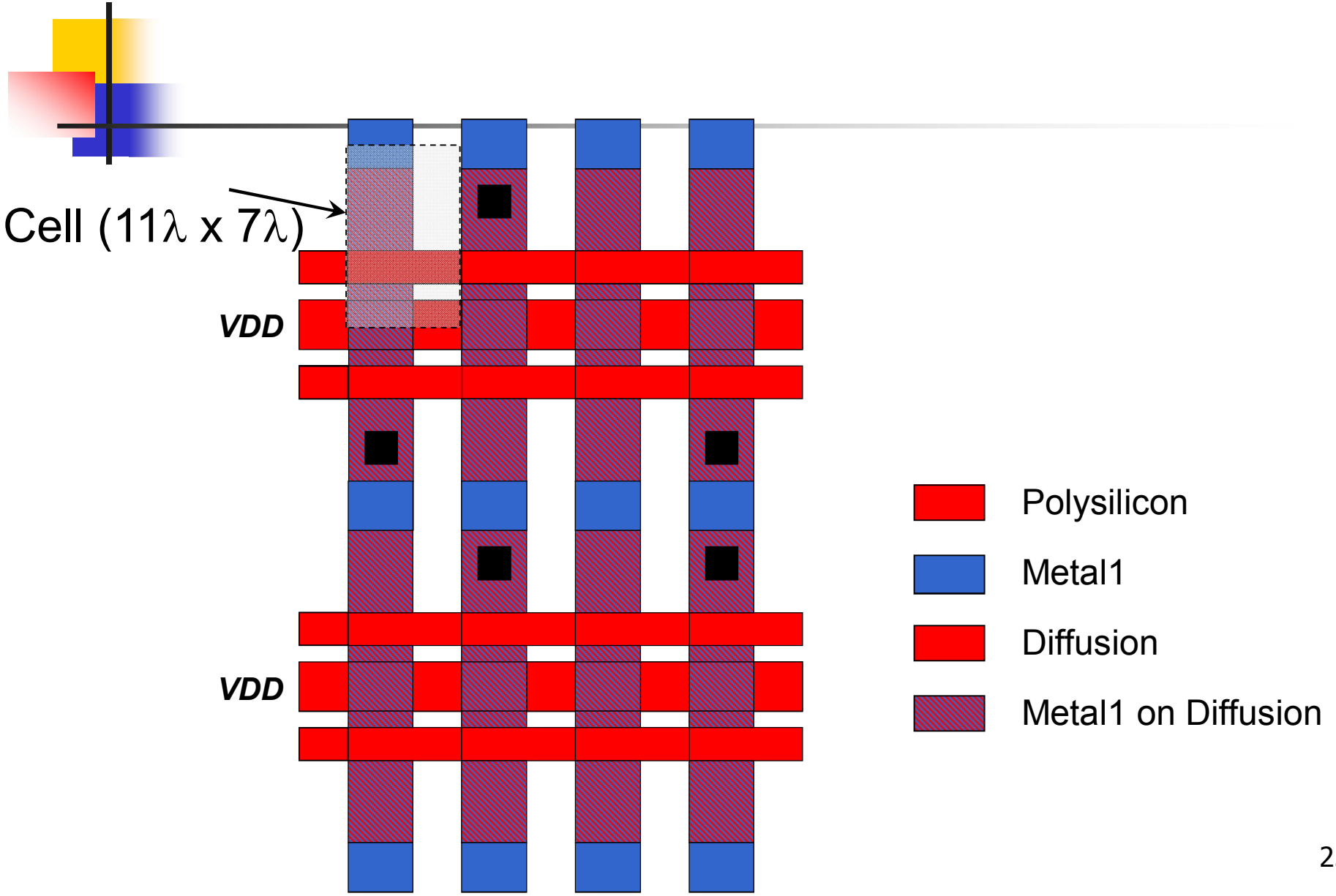
并联结构 ROM



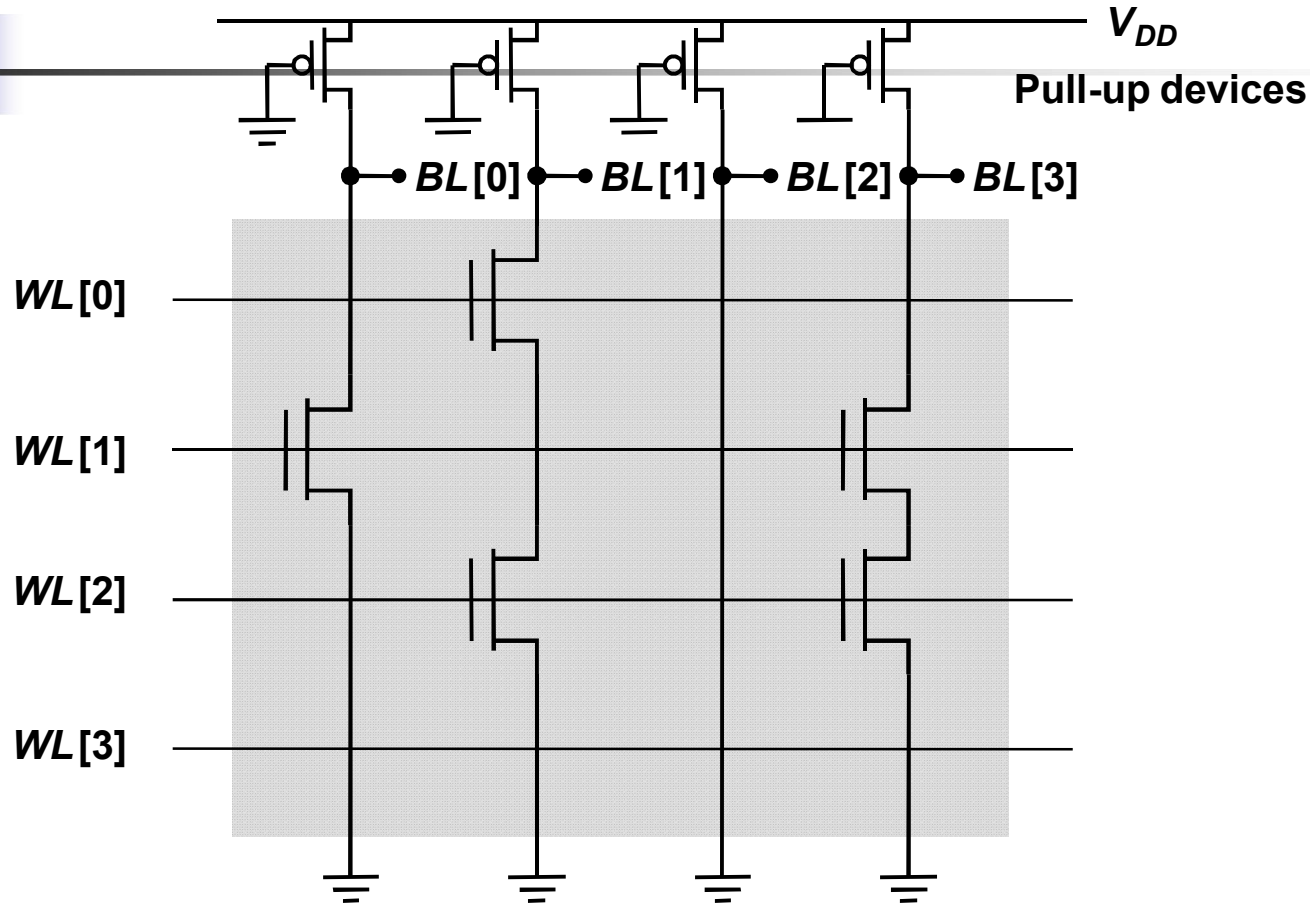
并联结构 ROM



并联结构 ROM 版图:接触孔编程



串并联结构 ROM



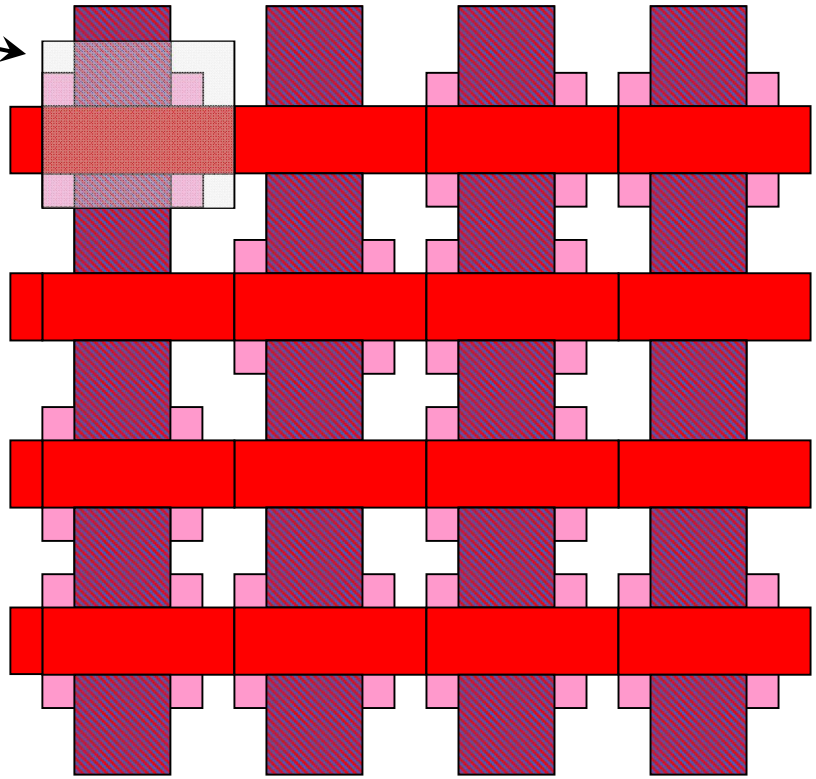
All word lines high by default with exception of selected row

只有选中字线的一行下拉，其他行维持上拉

串并联ROM 版图

No contact to VDD or GND necessary;
drastically reduced cell size
Loss in performance compared to NOR ROM

Cell (5λ x 6λ)



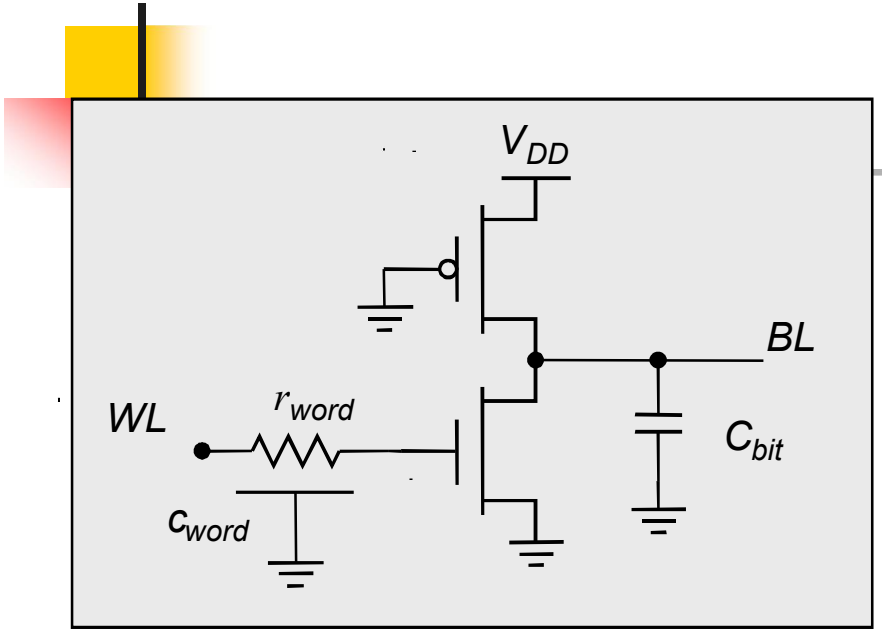
离子注入编程

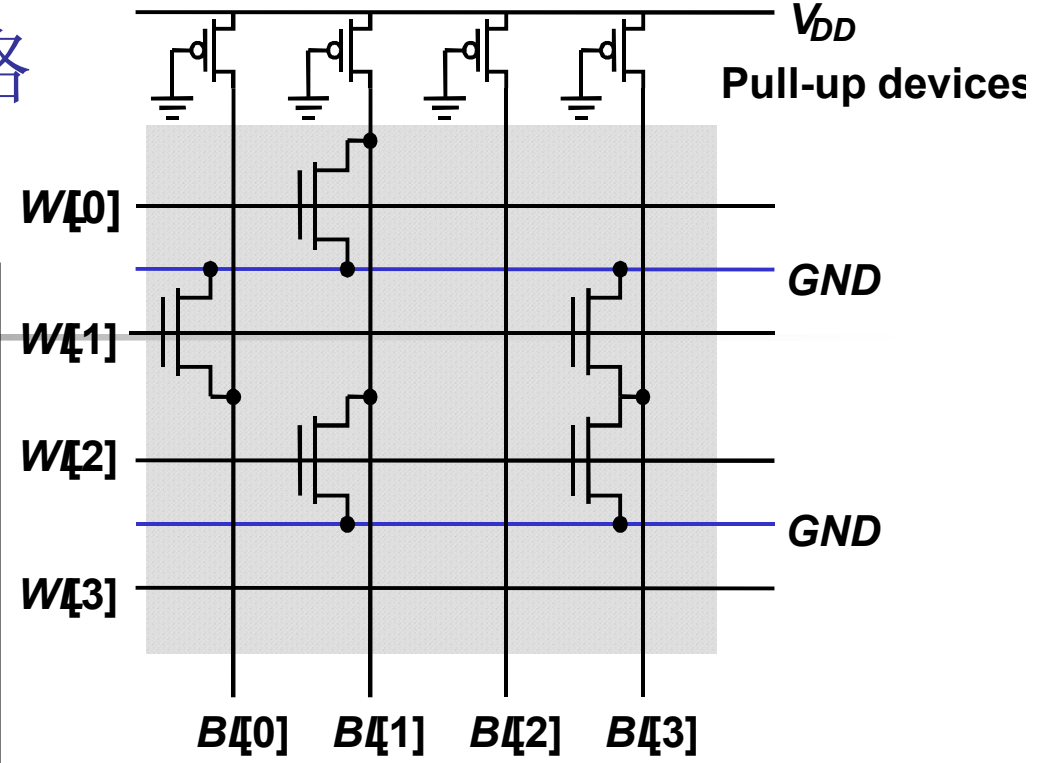
Polysilicon

Threshold-altering implant

Metal1 on Diffusion

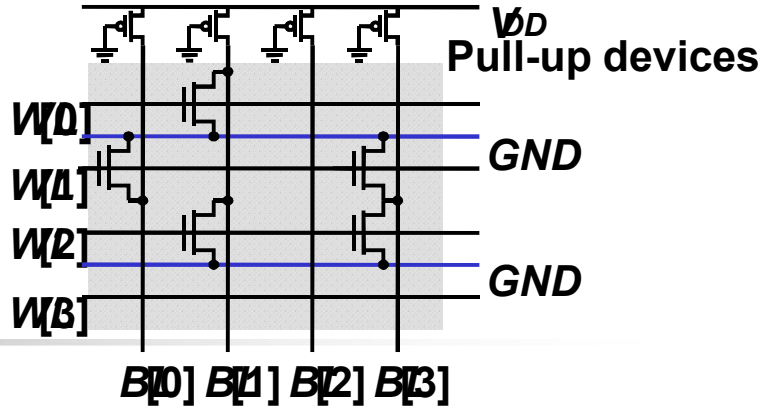
并联结构ROM等效电路





- 字线电容、电阻
  - Wire capacitance and gate capacitance
  - Wire resistance (polysilicon)
- 位线电容电阻
  - Resistance not dominant (metal)
  - Drain capacitance

减小字线延迟



Driver

WL Polysilicon word line

Metal word line

(a) Driving the word line from both sides

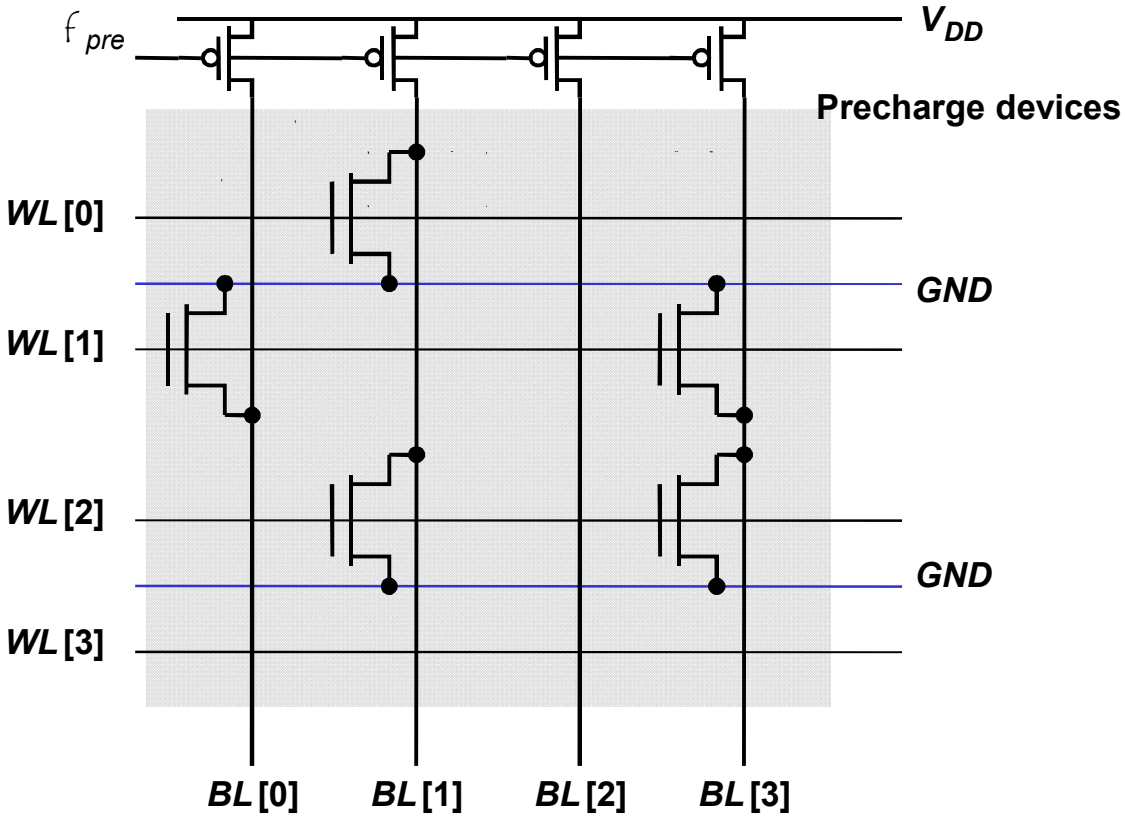
Metal bypass

WL *K* cells Polysilicon word line

(b) Using a metal bypass

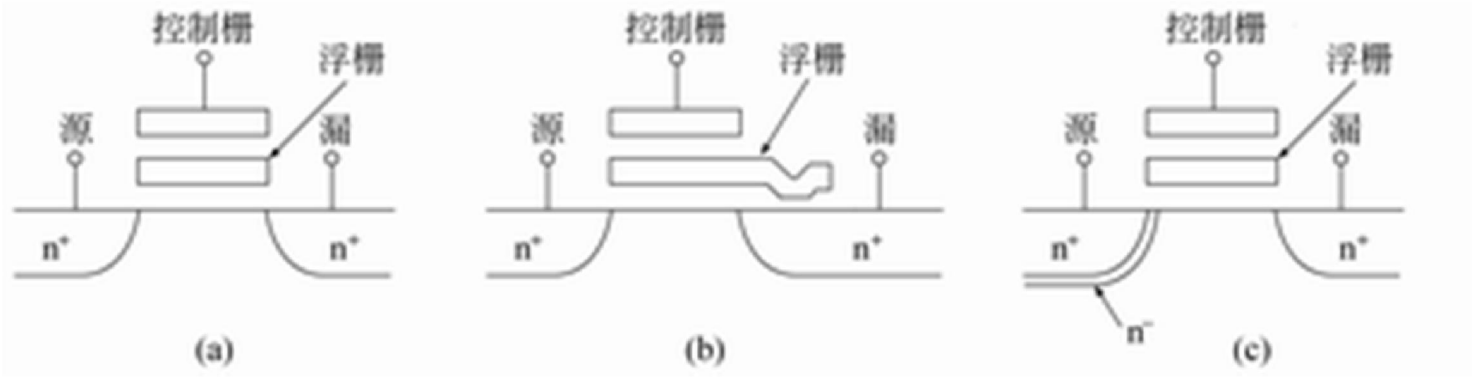
(c) Use silicides

Precharged MOS ROM



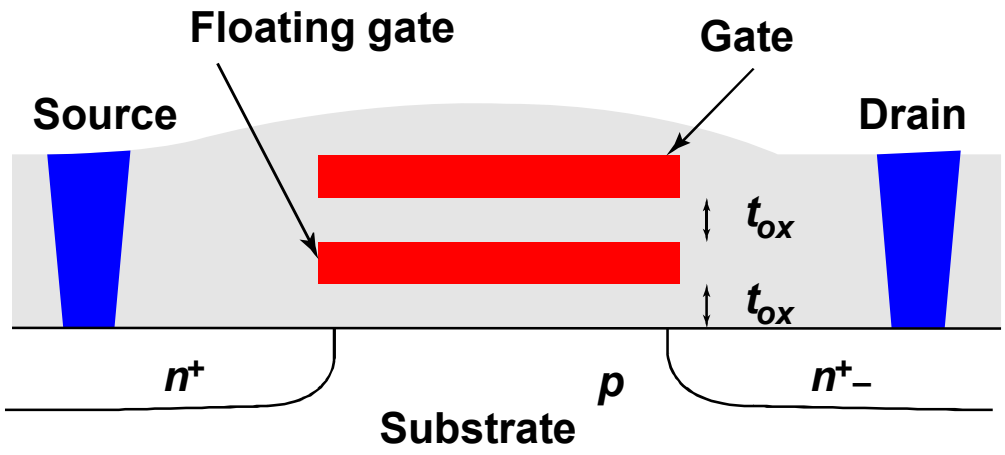
浮栅MOS管构成的EPROM

- 利用浮栅上的存储电荷改变**MOS**管的阈值电压

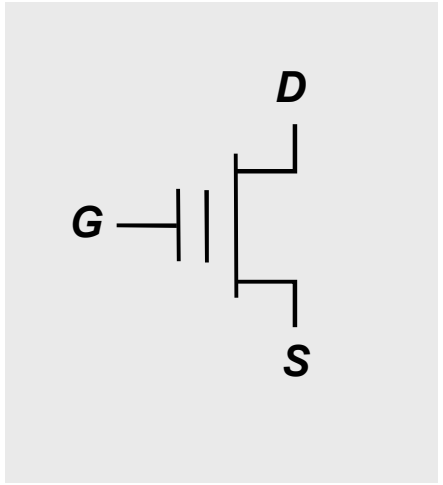


(a)EPROM (b)EEPROM (c)Flash

The Floating-gate transistor

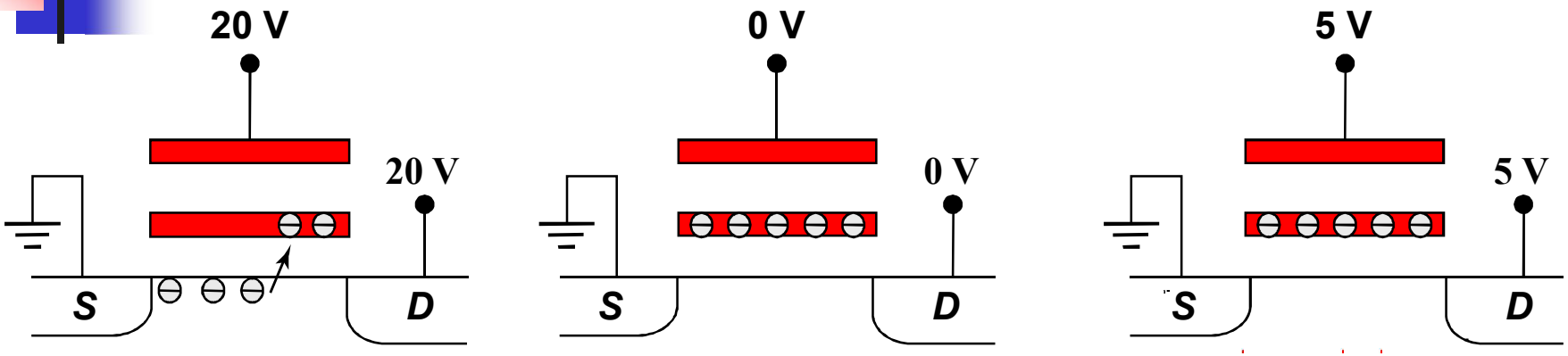


Device cross-section



Schematic symbol

Floating-Gate Transistor Programming

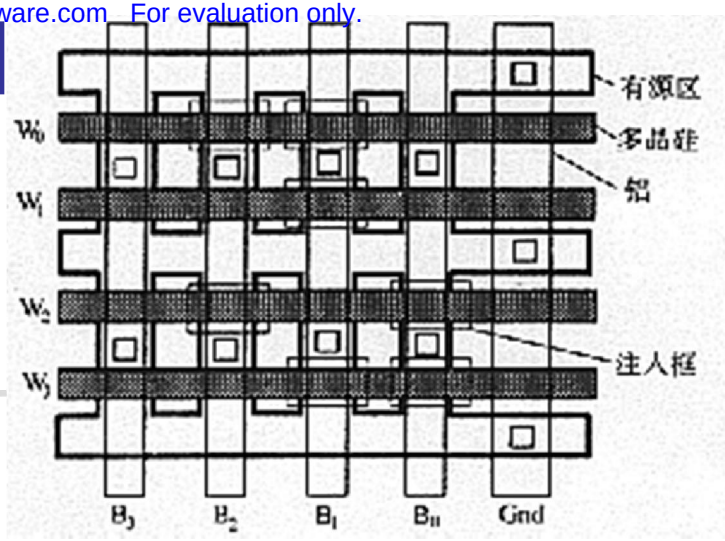


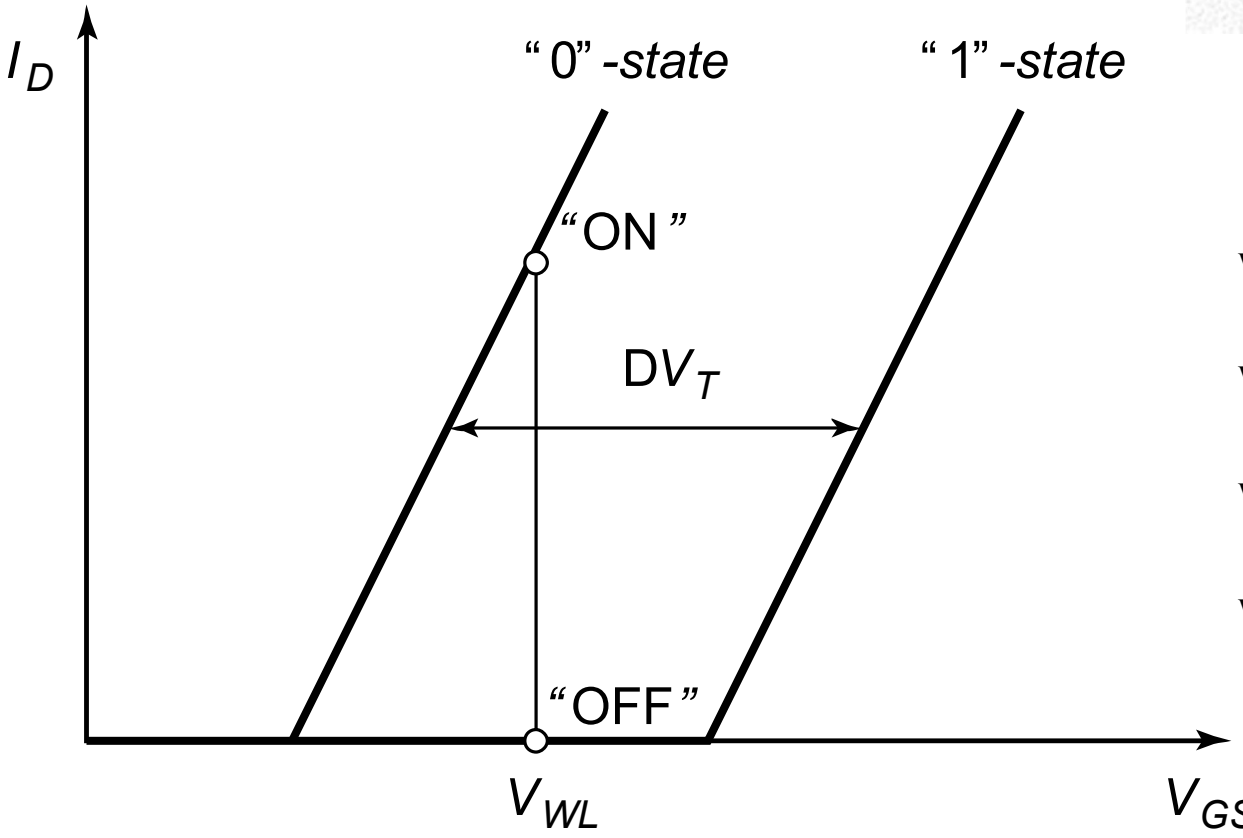
Avalanche injection

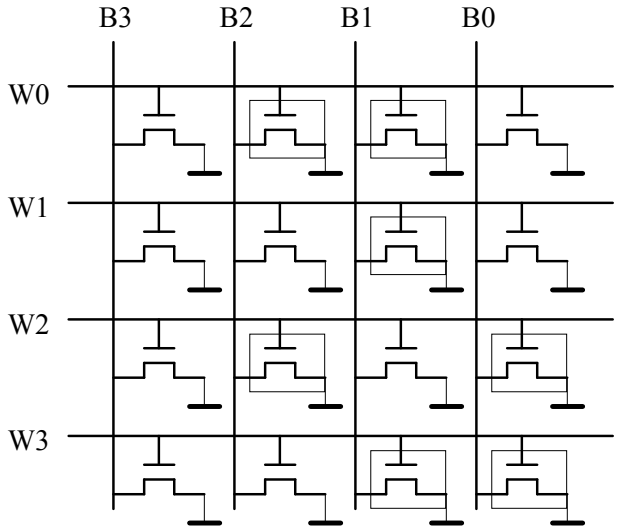
Removing programming voltage leaves charge trapped

Programming results in higher V_T.

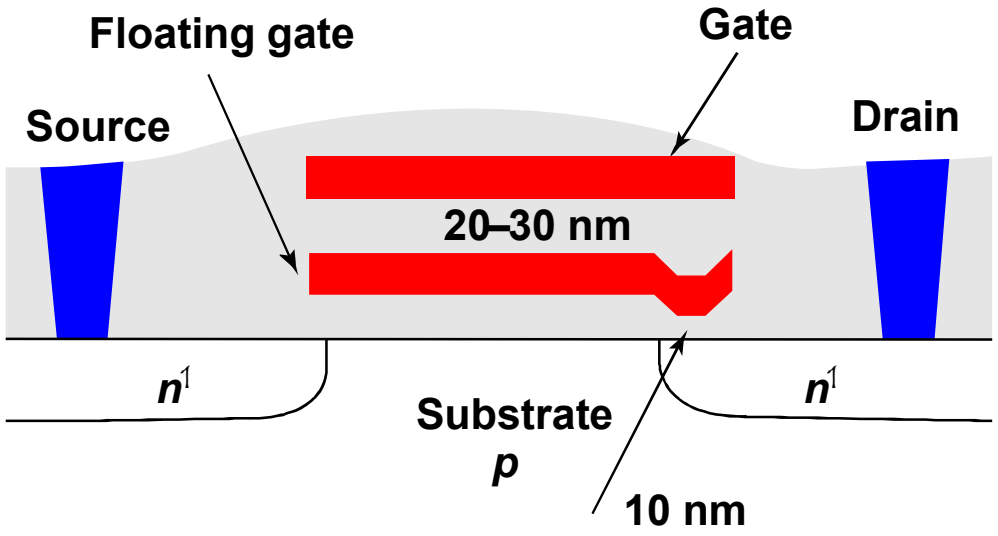
A "Programmable-Threshold Transistor



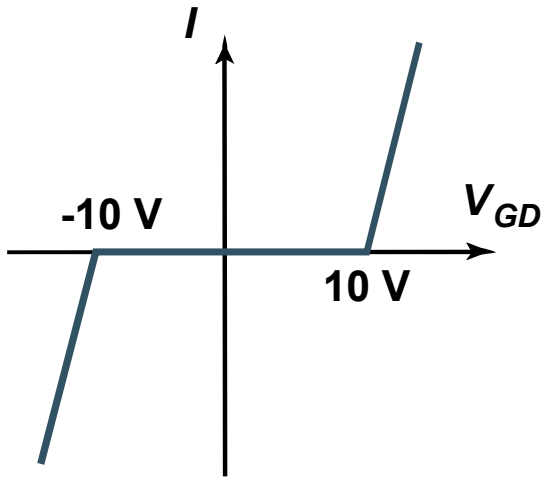




FLOTOX EEPROM

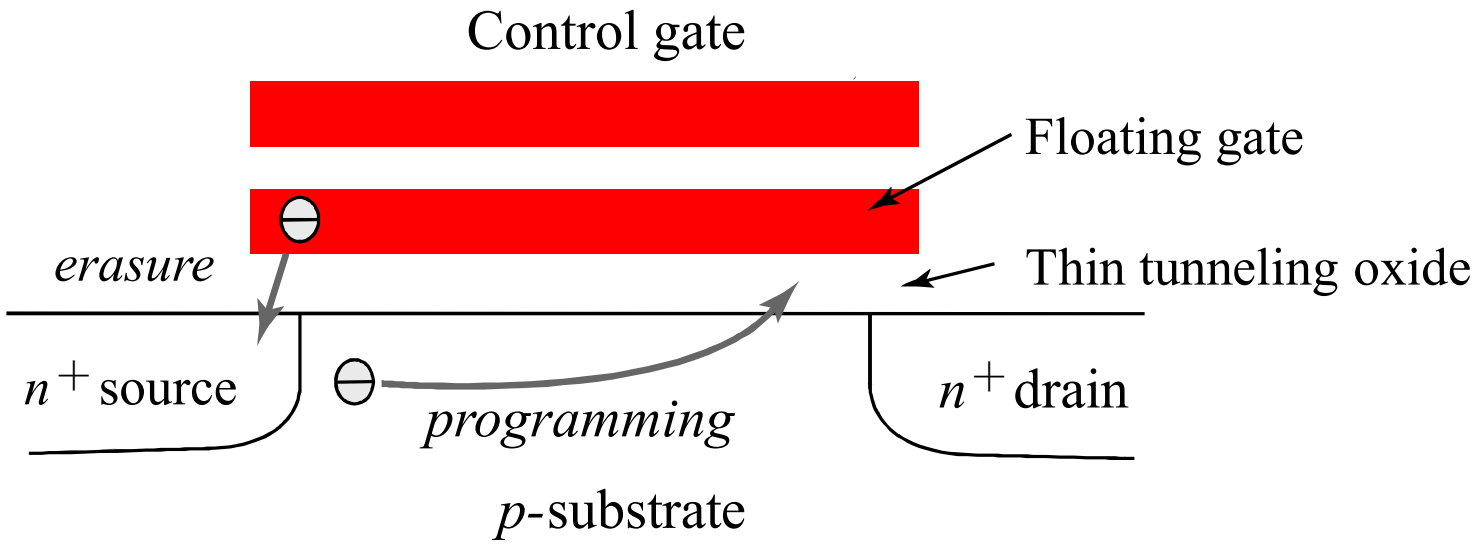


FLOTOX transistor



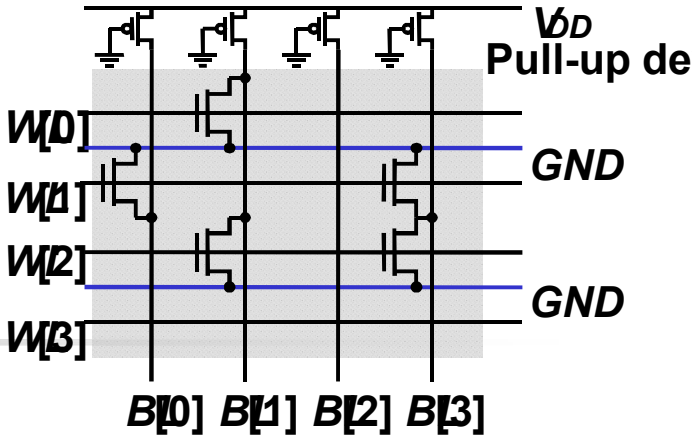
Fowler-Nordheim
I-V characteristic

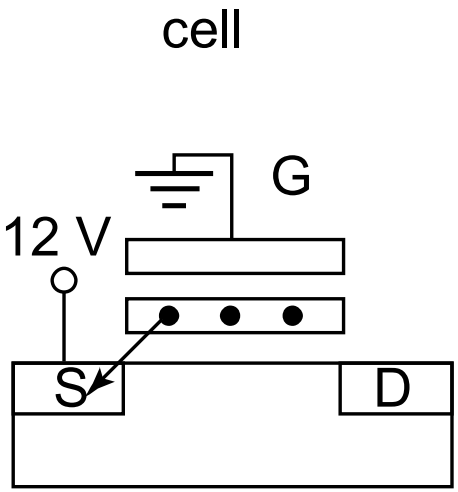
Flash EEPROM

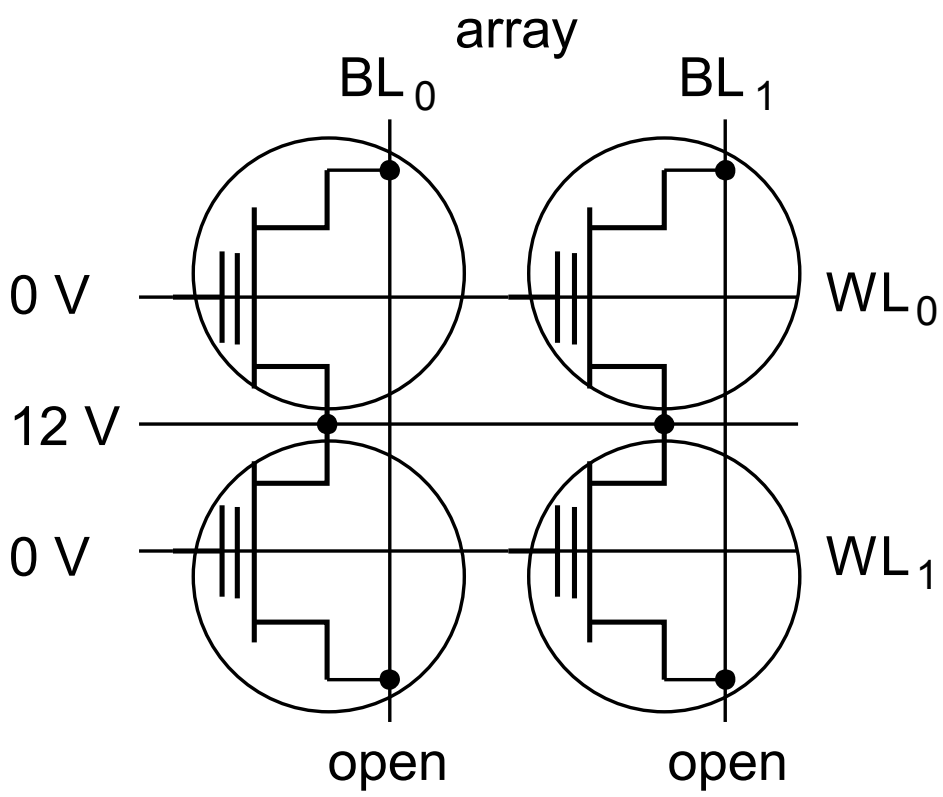


Many other options …

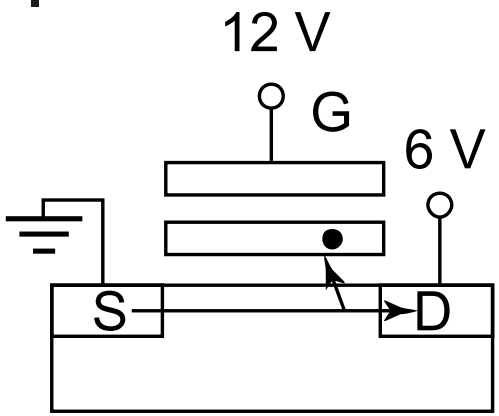
并联结构 Flash 的擦除过程

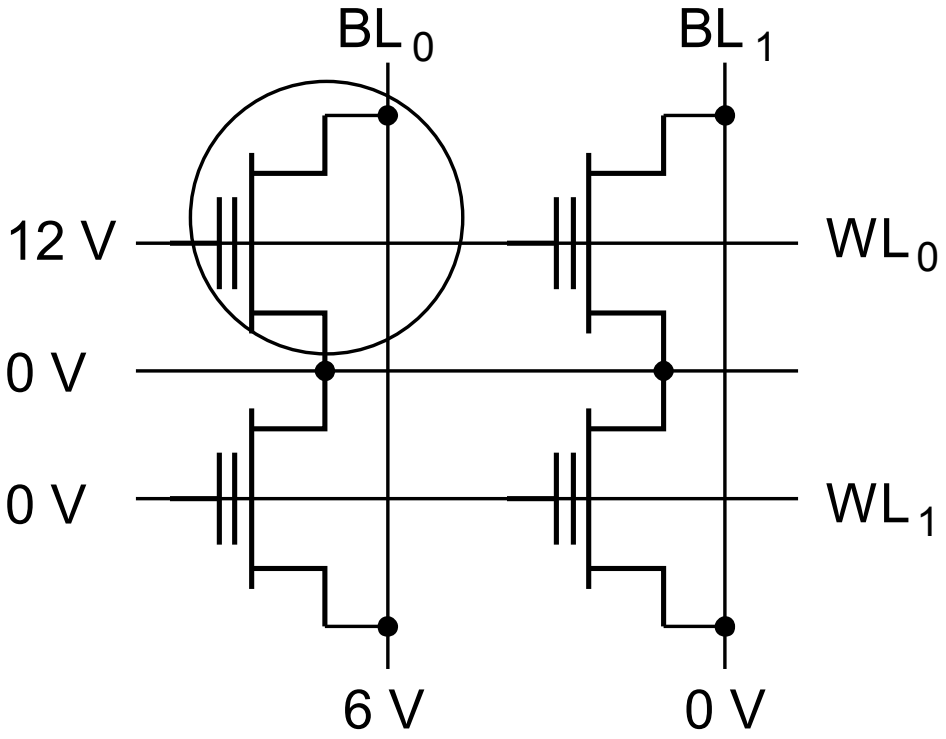




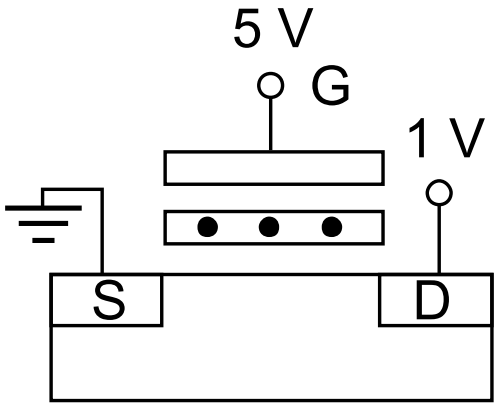


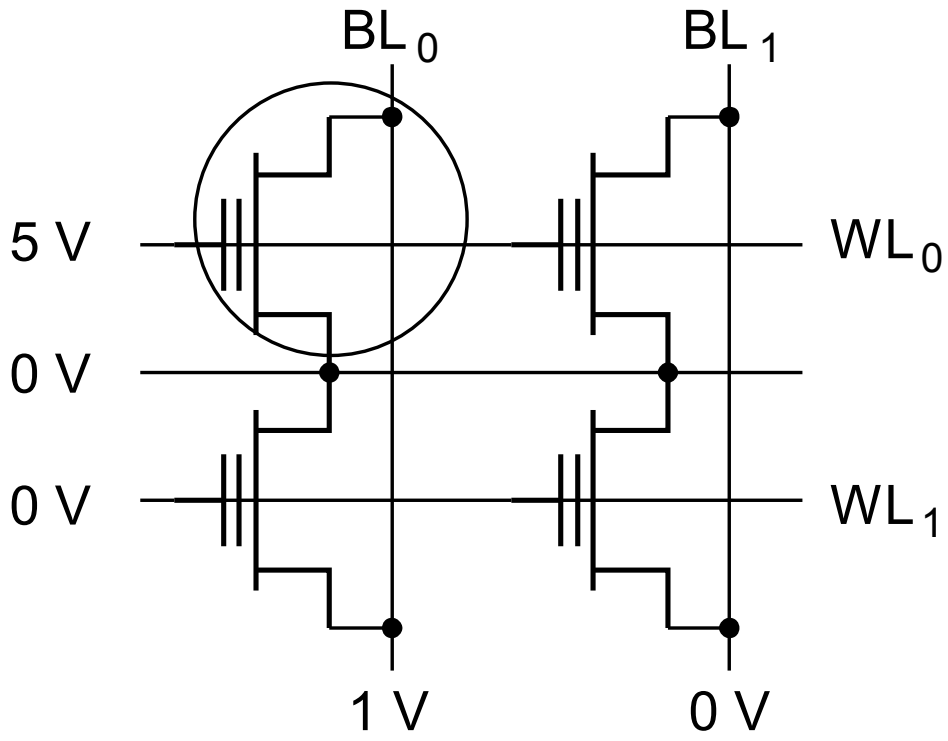
并联结构 Flash 写入过程



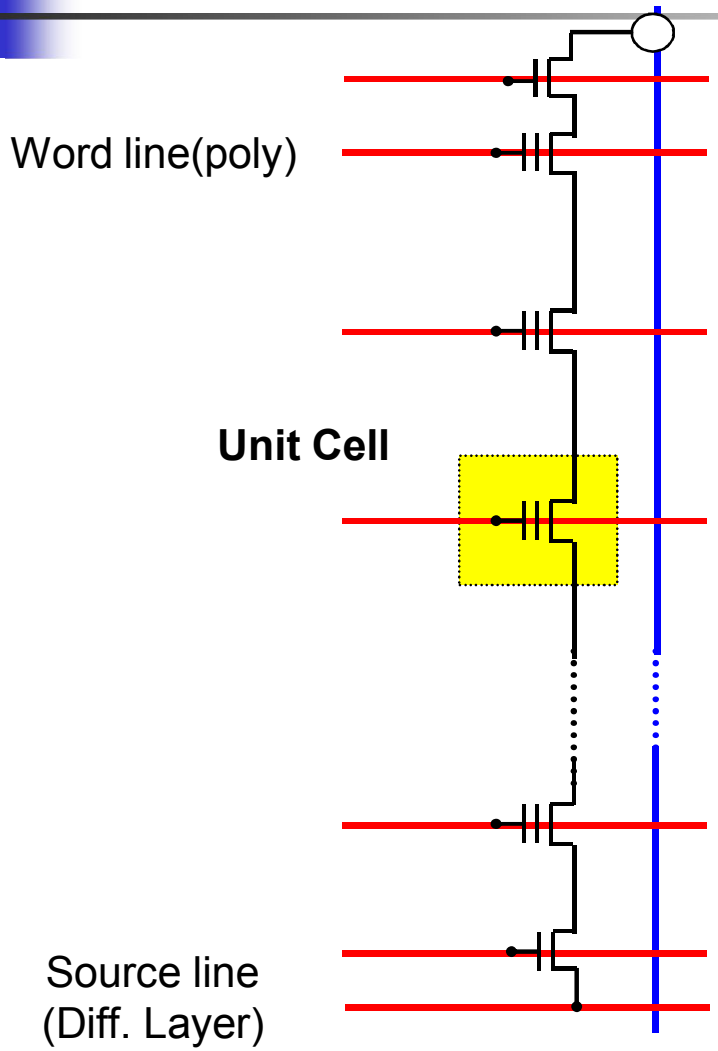


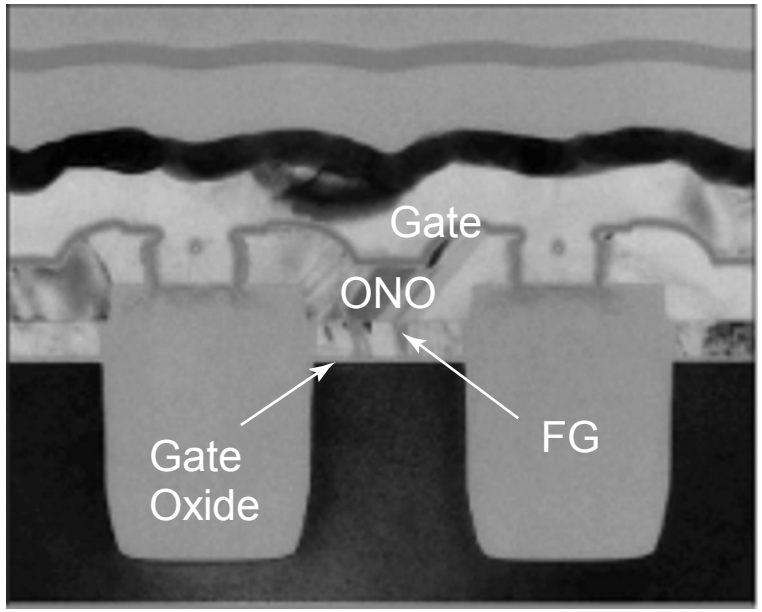
并联结构Flash的读出过程



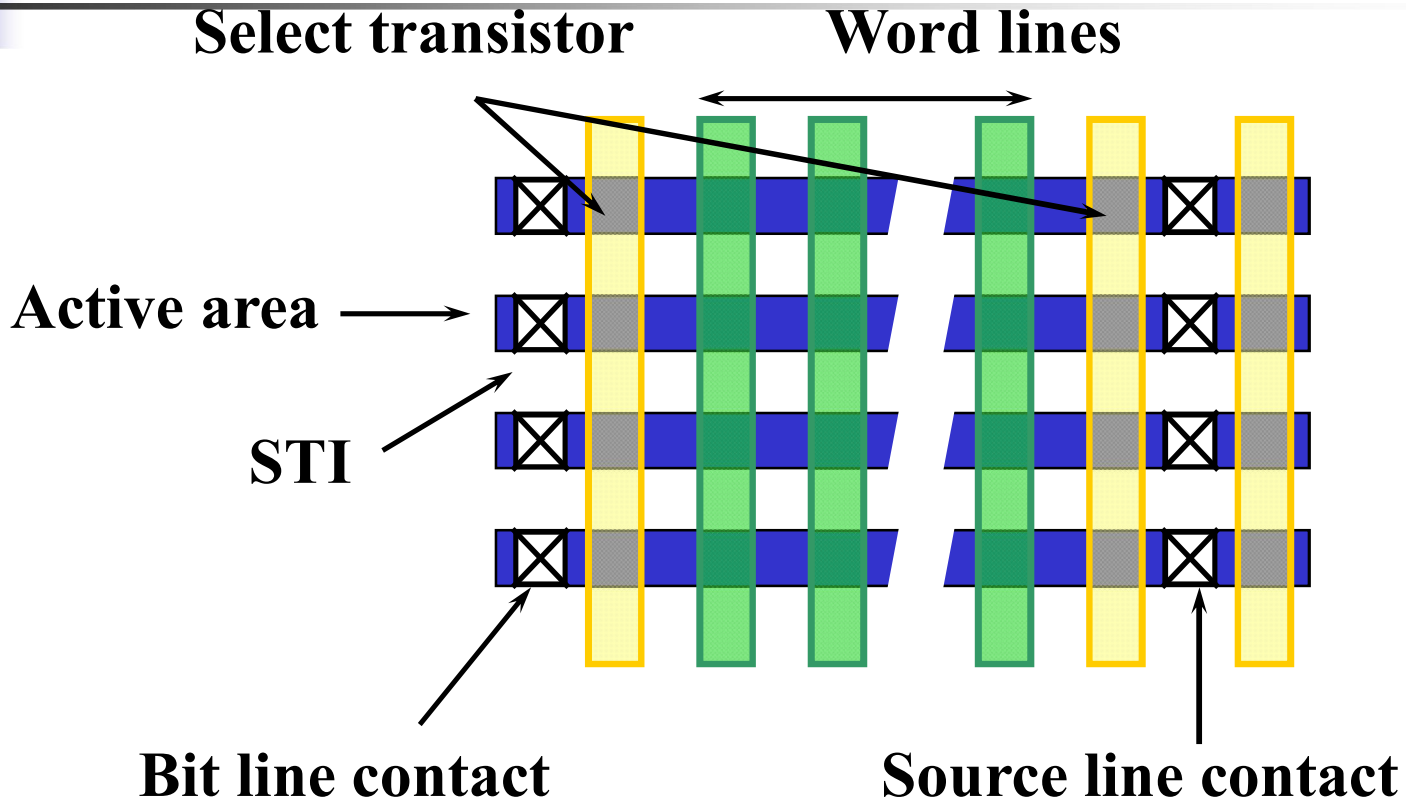


串联结构 Flash Memory





串联结构 Flash Memory



Courtesy Toshiba

Characteristics of ROM

Table 12-1 Comparison between nonvolatile memories ([Itoh01]).
V_{DD} = 3.3 or 5 V; V_{PP} = 12 or 12.5 V.

	Cell—Nr. of Transistors	Cell Area (ratio wrt EPROM)	Mechanism		External Power Supply		Program/ Erase Cycles
			Erase	Write	Write	Read	
MASK ROM	1 T (NAND)	0.35–5	—	—	—	V_{DD}	0
EPROM	1 T	1	UV Exposure	Hot electrons	V_{PP}	V_{DD}	~100
EEPROM	2 T	3–5	FN Tunneling	FN Tunneling	V_{PP} (int)	V_{DD}	10^4–10^5
Flash Memory	1 T	1–2	FN Tunneling	Hot electrons	V_{PP}	V_{DD}	10^4–10^5
			FN Tunneling	FN Tunneling	V_{PP} (int)	V_{DD}	10^4–10^5