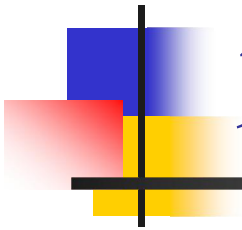
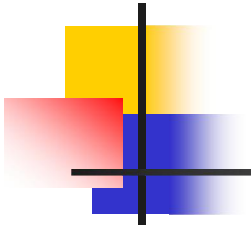


第四章 基本单元电路

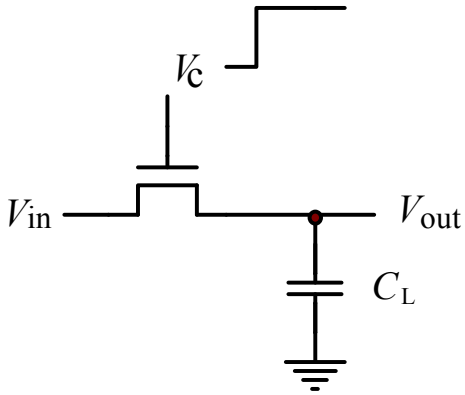
4.7 传输门基本特性



MOS传输门逻辑电路

- NMOS/PMOS传输门特性
- CMOS传输门特性
- 传输门的级联
- NMOS传输门的电平恢复

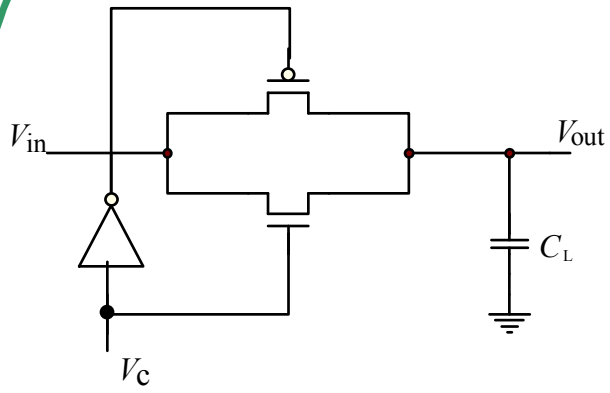
MOS传输门结构



NMOS传输门

Pass Transistor

源、漏端不固定
双向导通



CMOS传输门

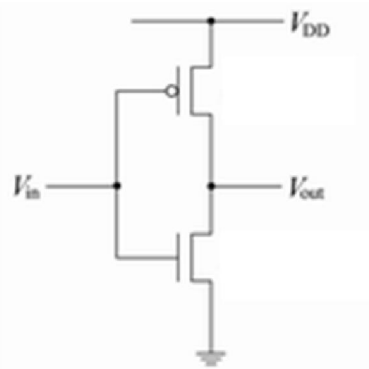
Transmission Gate

NMOS,PMOS并联

源、漏端不固定

栅极接相反信号

两管同时导通或
截止



CMOS反相器

NMOS,PMOS串联

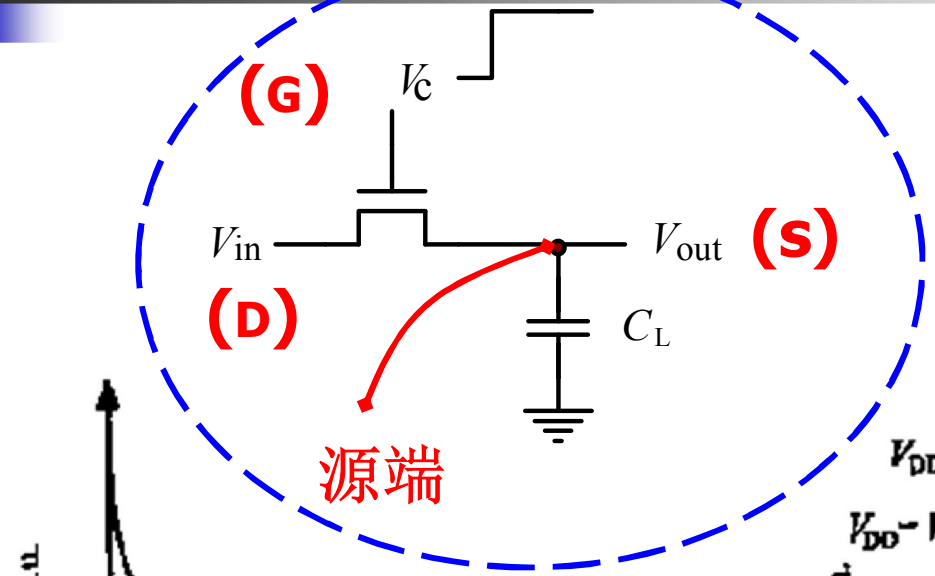
源端接固定电位、
漏端输出

栅极接相同信号

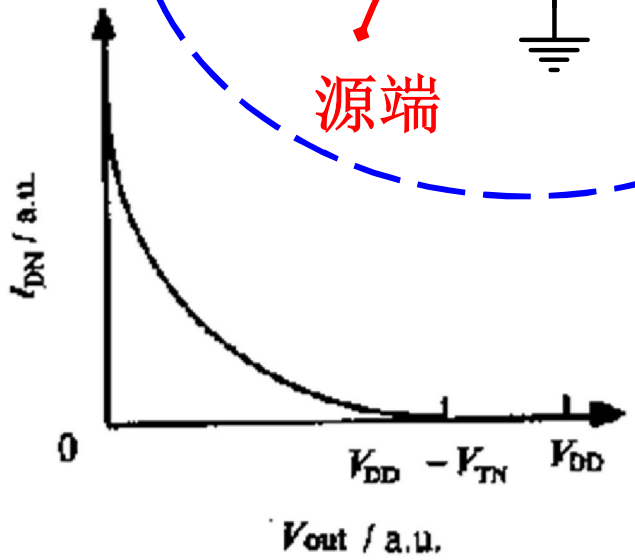
两管轮流导通或
截止

NMOS传输门传输高电平特性

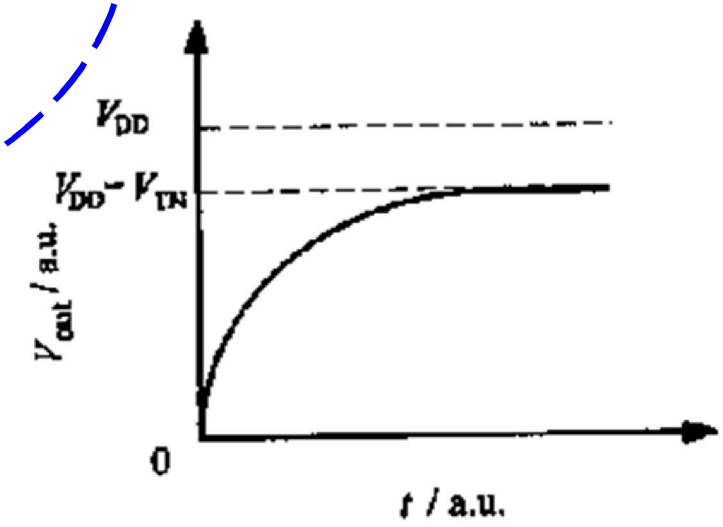
$V_{in}=V_{DD}, V_c=V_{DD}$



Hints: $V_D=V_G$, 器件始终处于饱和区，直到截止（类似于饱和负载的特性）

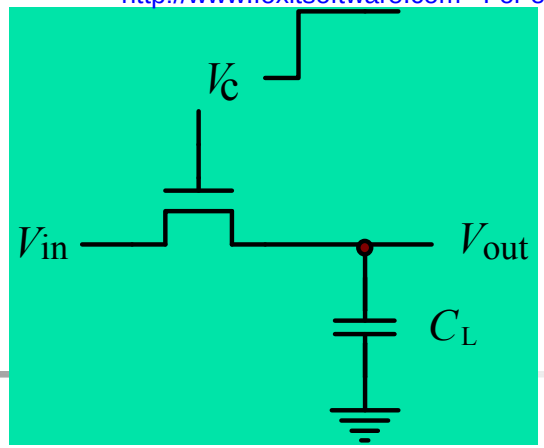


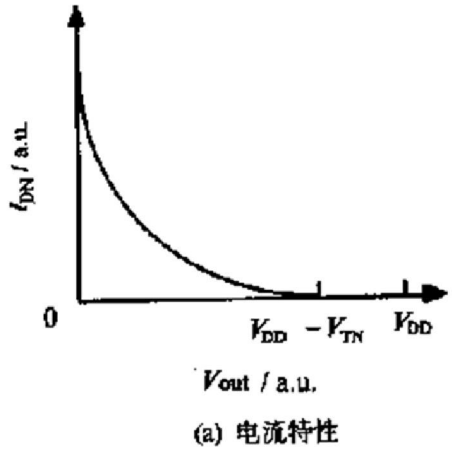
(a) 电流特性



(b) 输出电平的变化

NMOS传输高电平





- 输出电压：有阈值损失 $V_{in}=V_{DD}, V_c=V_{DD}$，$V_{out}=V_{DD}-V_{th}$
- 工作在饱和区，但是电流不恒定
- 衬偏效应

$$I_{DN}=K_N(V_{DD}-V_{TN}-V_{out})^2$$

  - 增加阈值损失
  - 减小电流

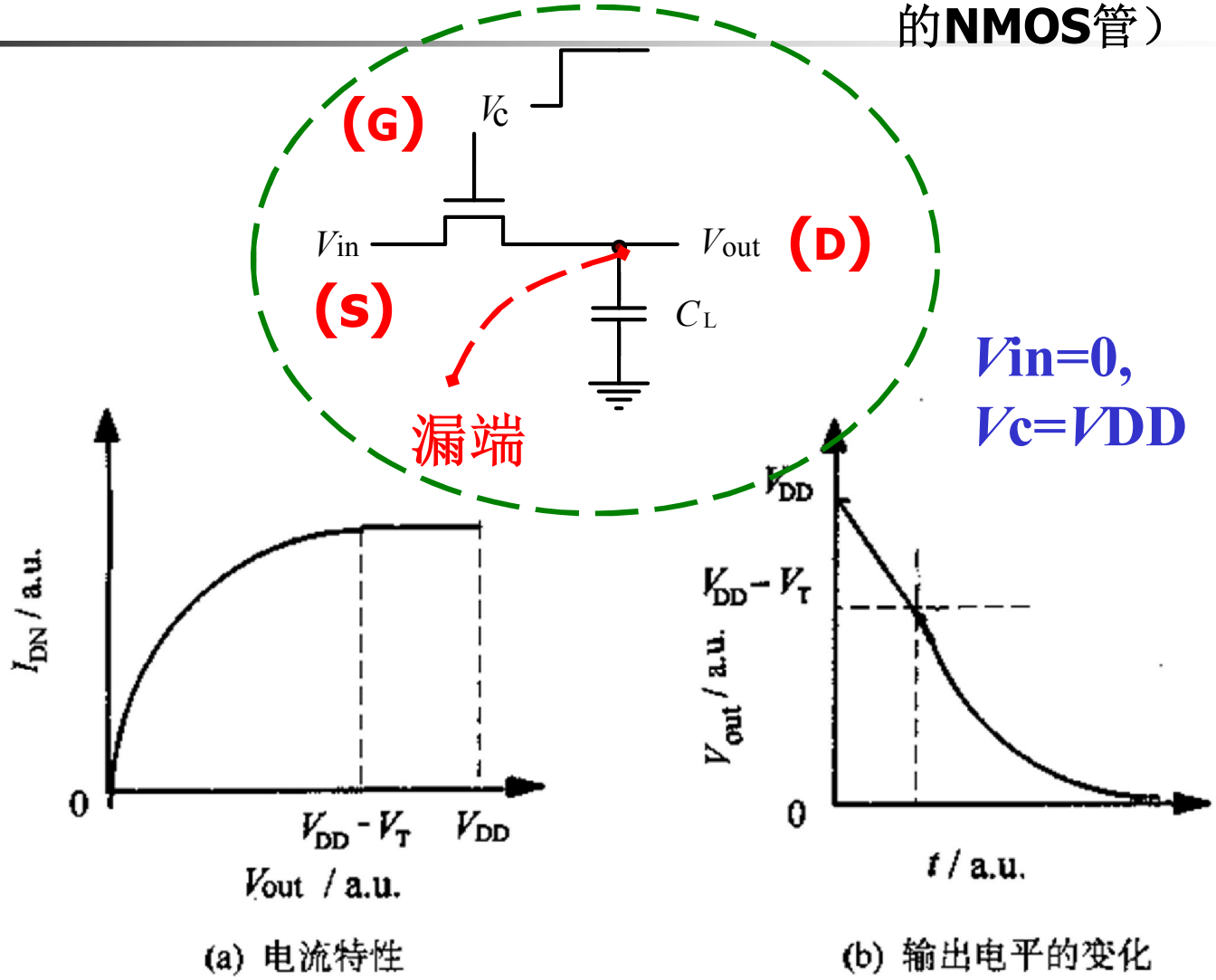
$$V_{TN}=V_{TN0}+\gamma(\sqrt{2\phi_f+V_{out}}-\sqrt{2\phi_f})$$

- 低效传输高电平(电平质量差，充电电流小)

NMOS传输门传输低电平特性

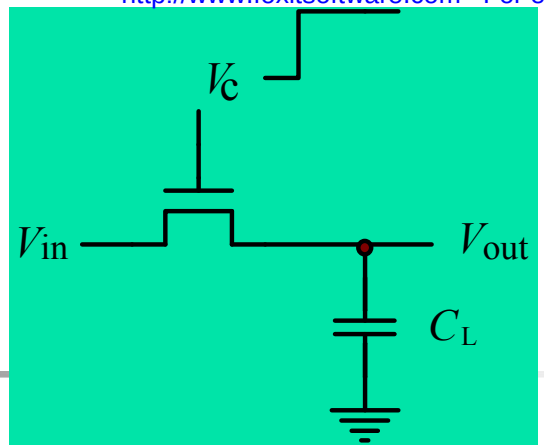
Hints:器件先处于饱和区后处于线性区

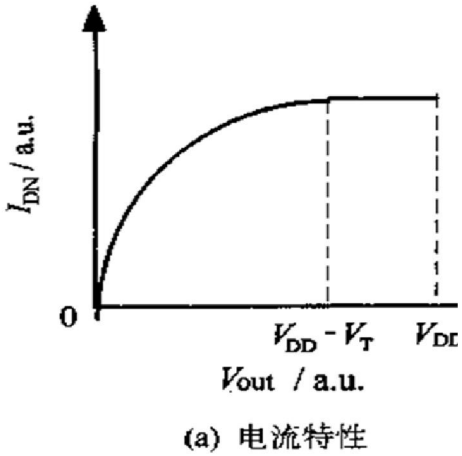
（类似于**CMOS**反相器中的**NMOS**管）



(a) 电流特性　　(b) 输出电平的变化

NMOS传输低电平



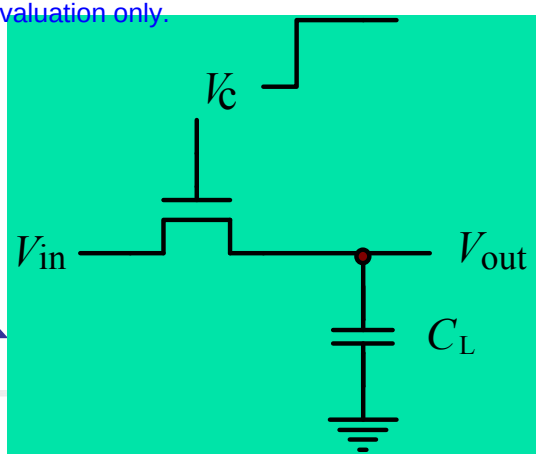


(a) 电流特性

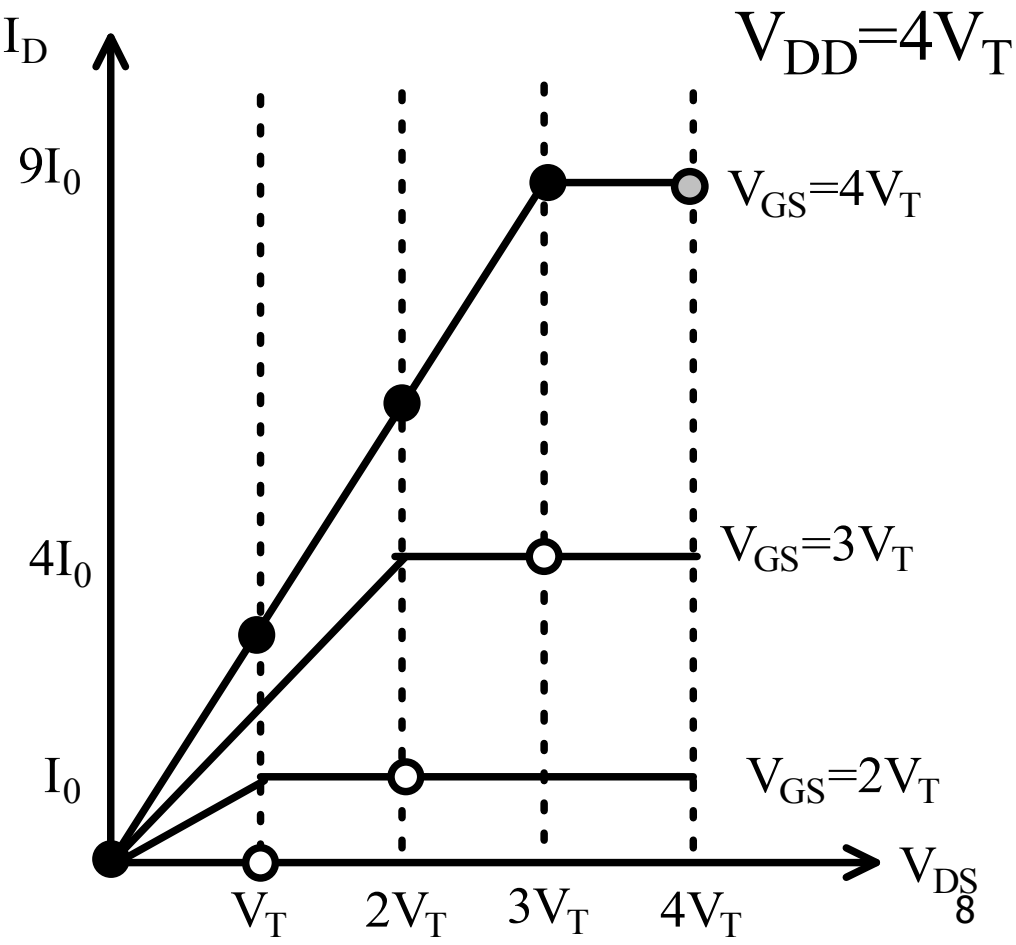
- 输出电压：没有阈值损失 $V_{in}=0, V_c=V_{DD}$，$V_{out}=0$
- 先工作在饱和区，后进入线形区
- 没有衬偏效应 $$I_{DN1} = K_N (V_{DD} - V_{TN})^2$$
- 高效传输低电平 $$I_{DN2} = 2K_N (V_{DD} - V_{TN}) V_{out}$$

（电平质量好，充电电流大）

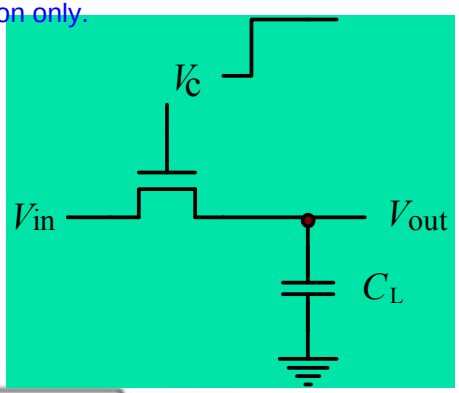
NMOS传输门等效电阻

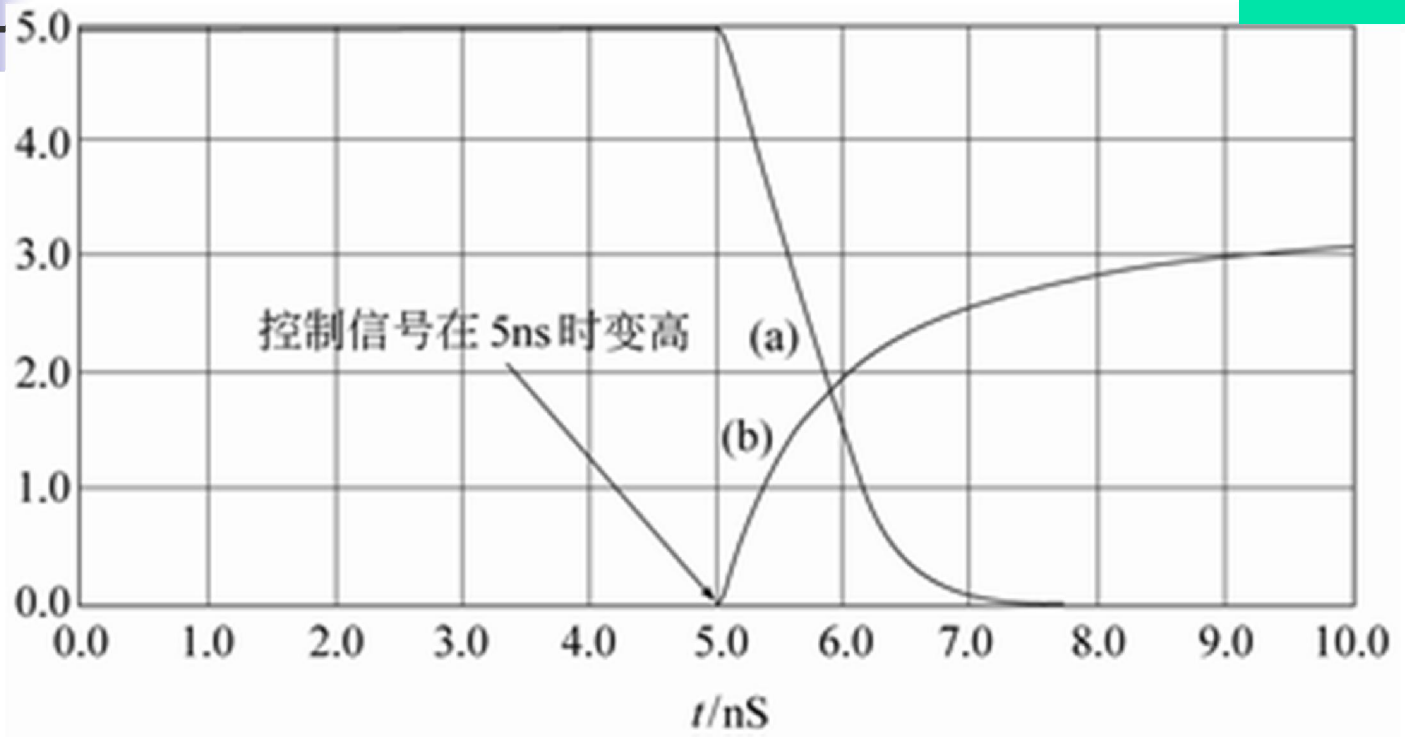


- 估算**NMOS**传输门等效电阻
- 传输低电平（深颜色点），传输高电平（浅颜色点）
- 分别求出平均电阻
- 传输高电平等效电阻约为低电平**2—3**倍



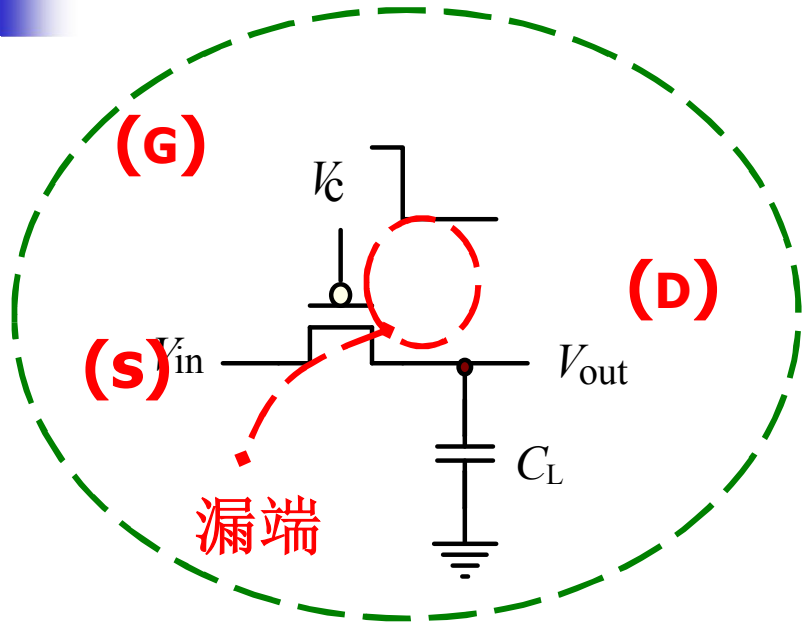
NMOS传输高电平和低电平





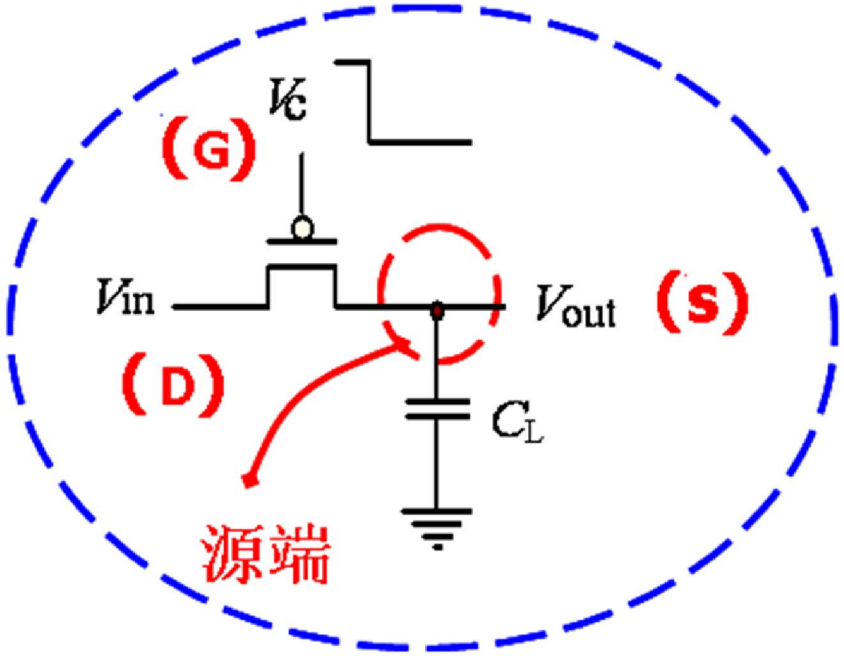
- 由于工作状态不同，以及衬偏效应的影响
- NMOS传输高电平过程的等效电阻近似为传输低电平时的2-3倍

PMOS传输门传输特性



传输高电平情况

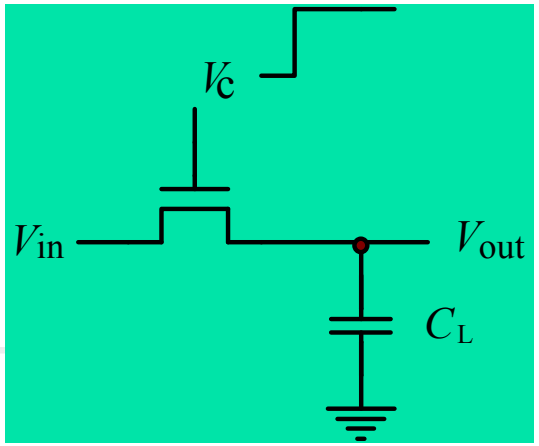
器件先处于饱和区，
后处于线性区



传输低电平情况

器件始终处于饱和区，
直到截止

NMOS/PMOS传输门：RC延迟



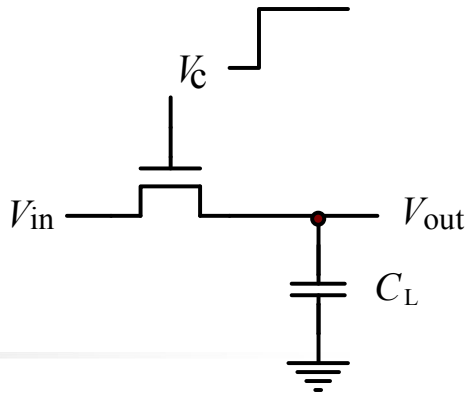
- 沿用反相器部分的分析模型，宽度为**W**的**PMOS**导电因子为**K0**，等效电阻为**R0**，漏电容为**C0**，并有迁移率**2**倍近似
- 如果负载电容只有传输管的漏电容，则宽度为**W/2**的**NMOS**的传输延迟：

$$t_{pHL} \propto \frac{1}{4} R_0 C_0$$

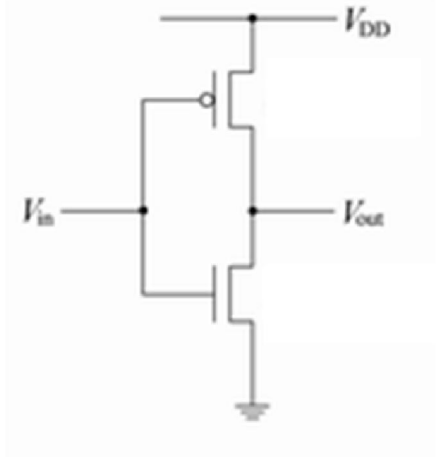
- 多级串联的传输门可以根据集总或者**elmore**模型计算

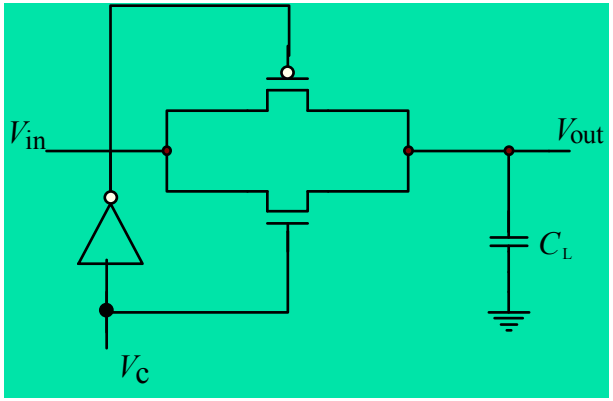
$$t_{pLH} \propto \frac{1}{2} R_0 C_0$$

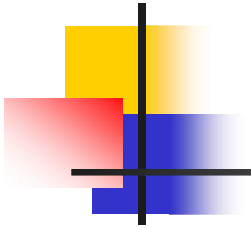
传输管（NMOS/PMOS传输门）



- 结构简单
- 有阈值损失
- **NMOS高效传输低电平，低效传输高电平**
- **PMOS载流子迁移率小，NMOS传输门应用更多**



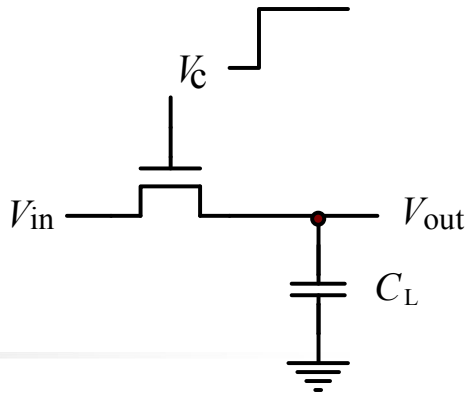


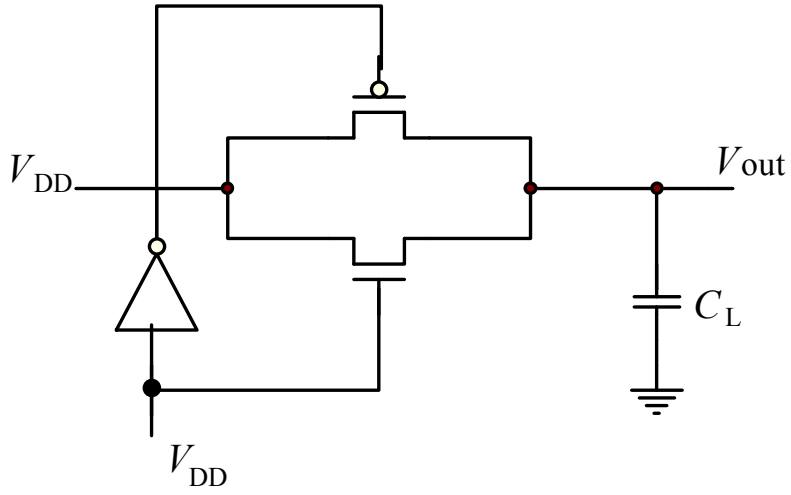


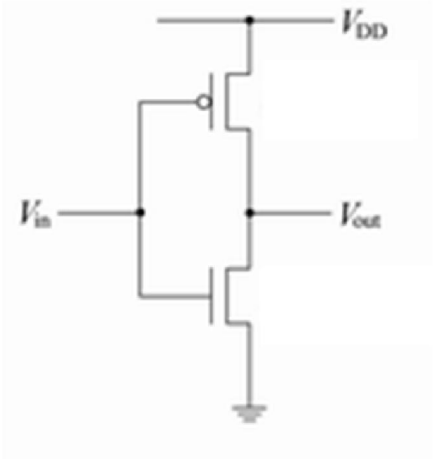
MOS传输门逻辑电路

- **NMOS/PMOS传输门特性**
- **CMOS传输门特性**
- 传输门的级联
- **NMOS传输门的电平恢复**

CMOS传输门传输高电平特性







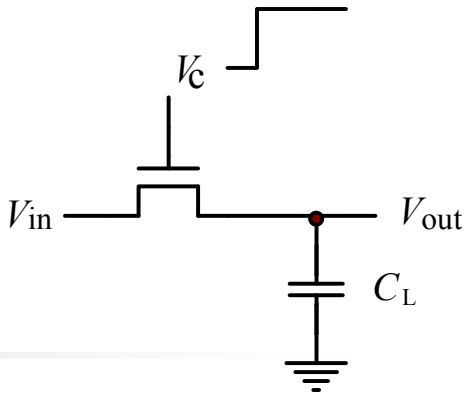
传输高电平分为3个阶段：

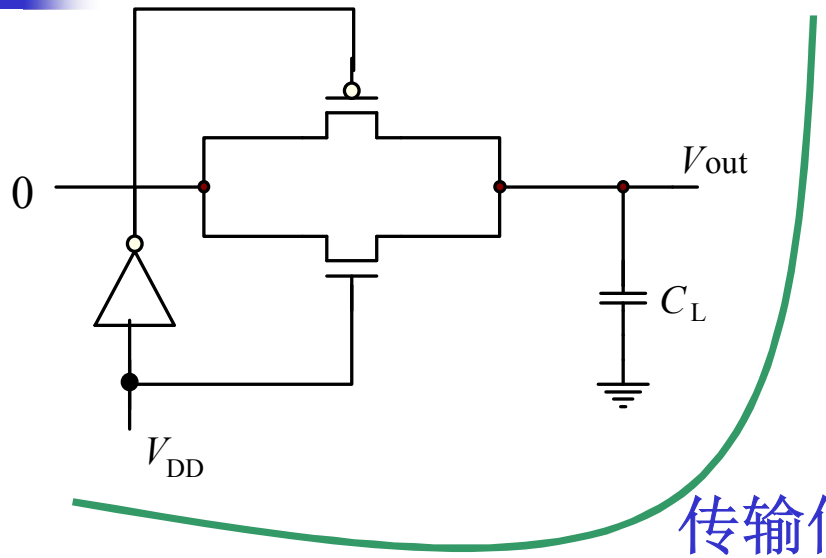
（1）$V_{out} \le -V_{TP}$， **NMOS和PMOS都饱和；**

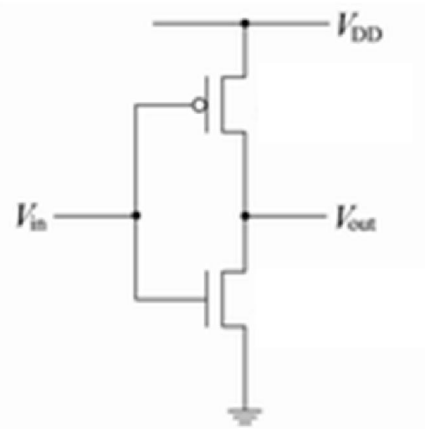
（2）$-V_{TP} < V_{out} < V_{DD} - V_{TN}$，**NMOS饱和,PMOS线性；**

（3）$V_{out} \ge V_{DD} - V_{TN}$， **NMOS截止,PMOS线性。**

CMOS传输门传输低电平特性







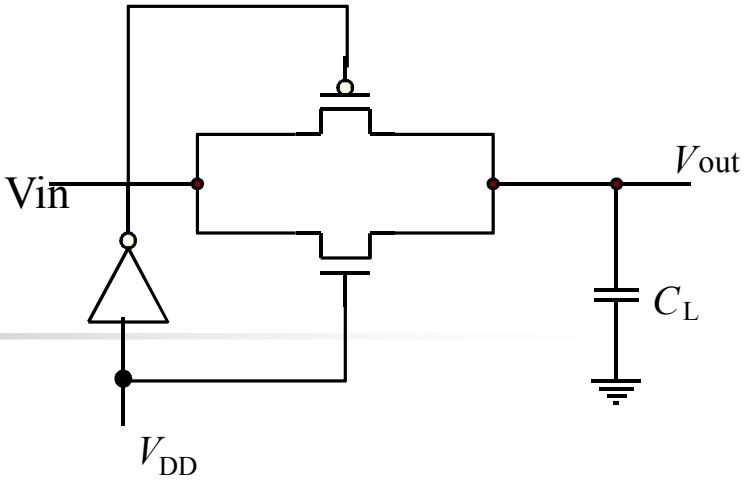
传输低电平分为3个阶段：

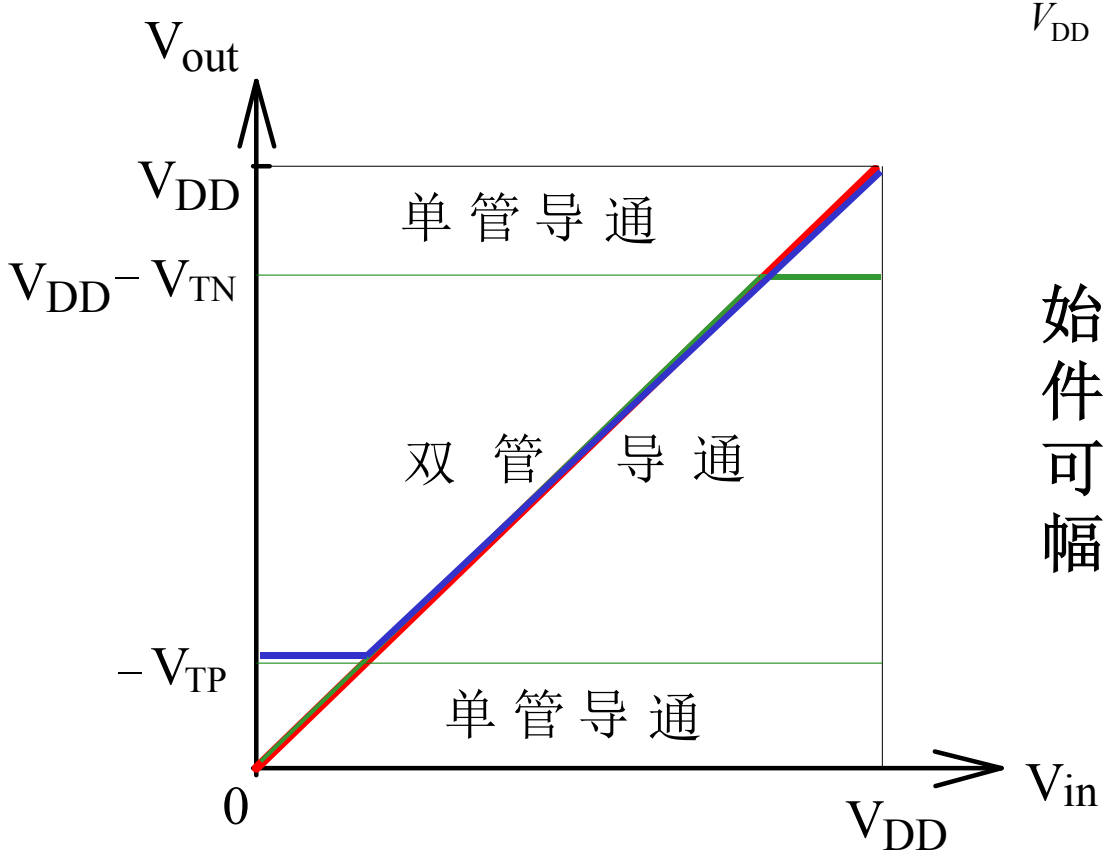
（1） $V_{out} \geq V_{DD} - V_{TN}$， **NMOS和PMOS都饱和；**

（2） $V_{DD} - V_{TN} > V_{out} > -V_{TP}$， **NMOS线性,PMOS饱和；**

（3） $V_{out} \leq -V_{TP}$， **NMOS线性,PMOS截止。**

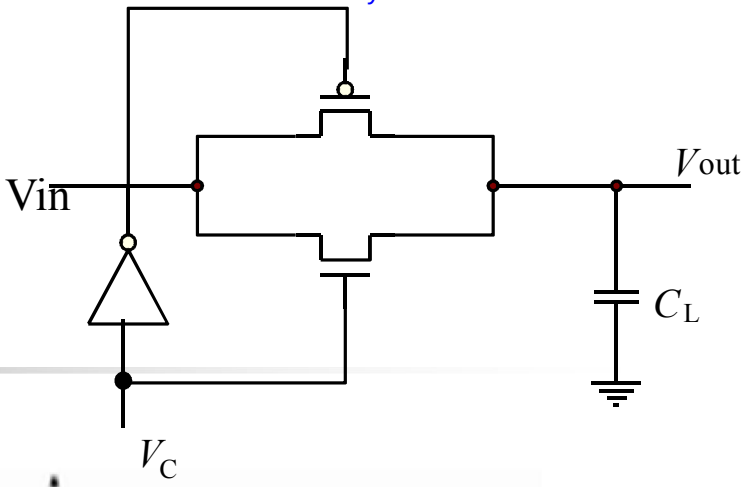
CMOS传输门直流电压传输特性

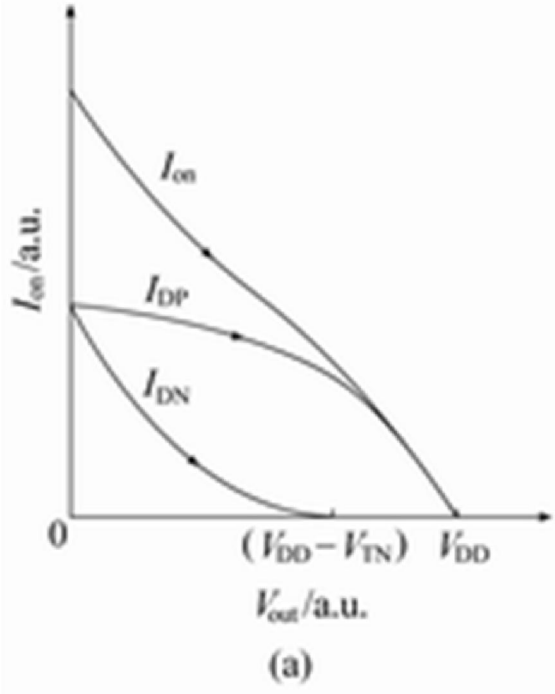


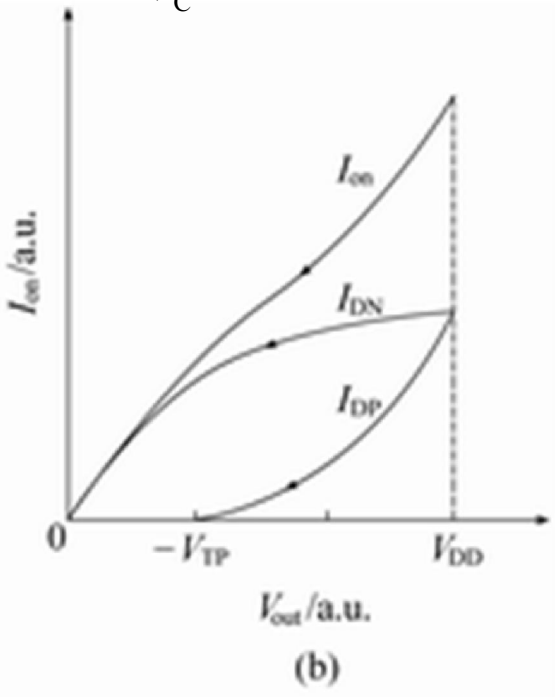


始终有一个器件是导通的，可以传输全摆幅的信号

CMOS传输门导通电流的变化



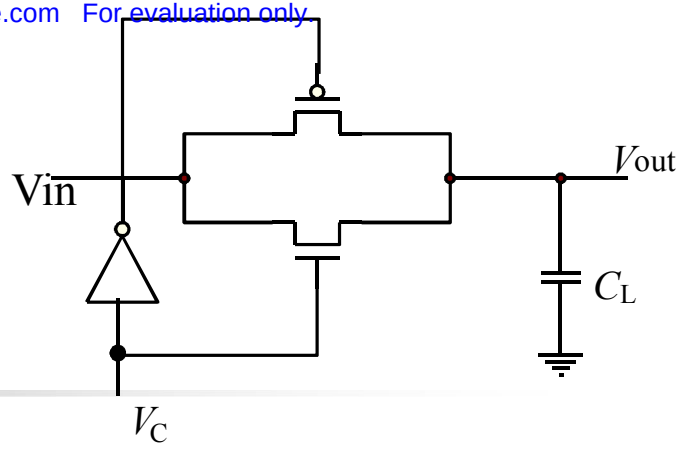




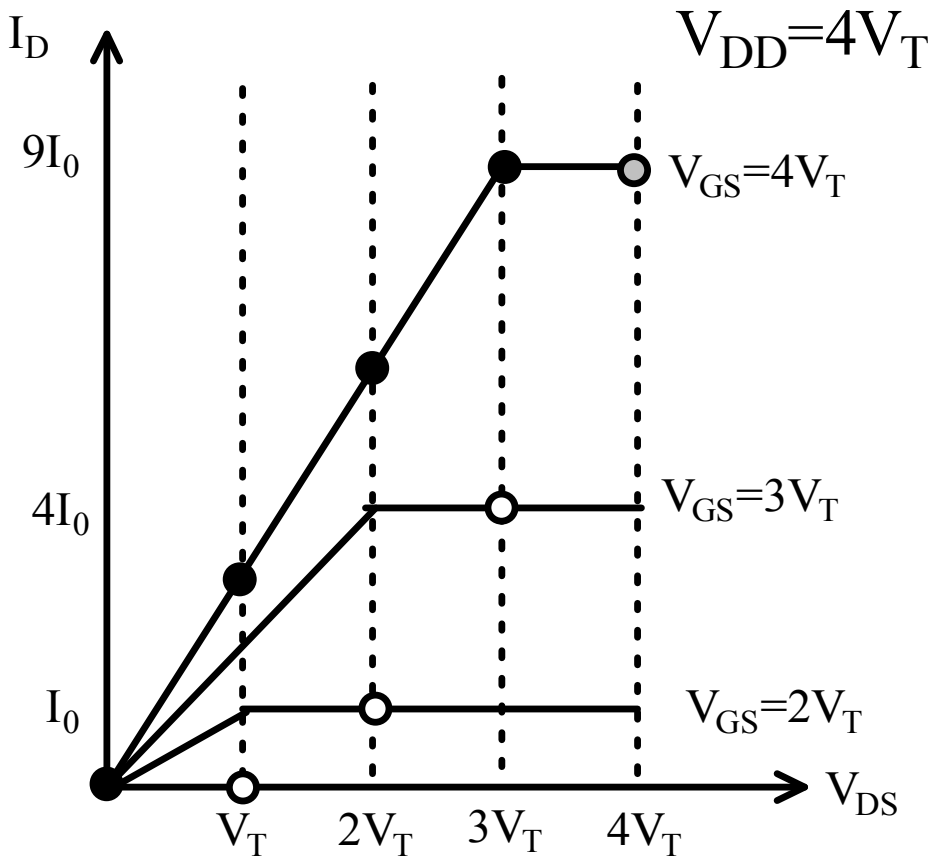
传输高电平

传输低电平

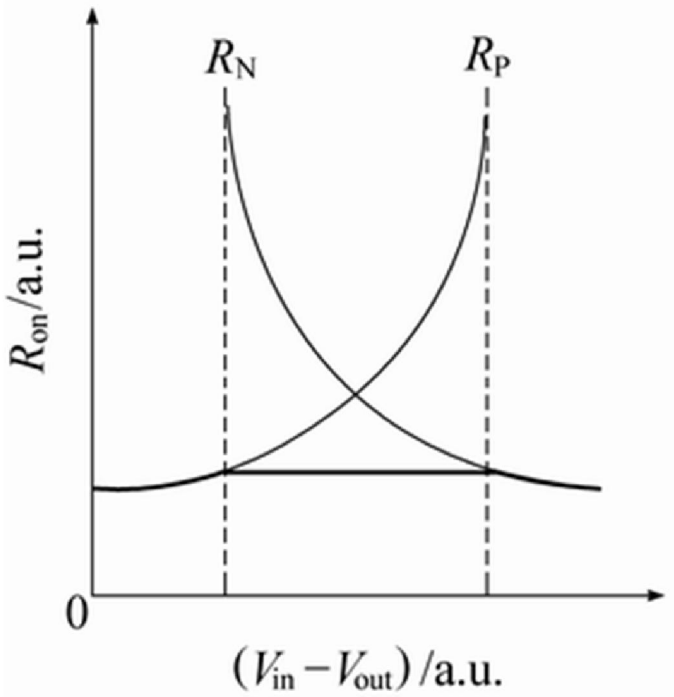
CMOS传输门导通电流



- 假设**CMOS**传输门的器件阈值电压和导电因子均相等，并忽略衬偏
- 高效传输（深颜色点），低效传输（浅颜色点）
- 二者之和为**CMOS**传输门导通电流
- 电流随**Vds**近似线性变化



CMOS传输门导通电阻的变化



传输延迟时间

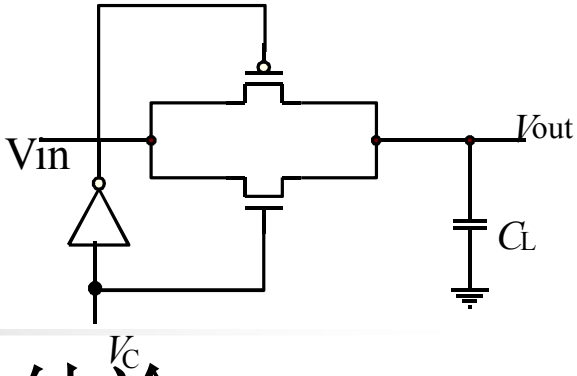
$$t_p = R_{on}C_L$$

传输低电平

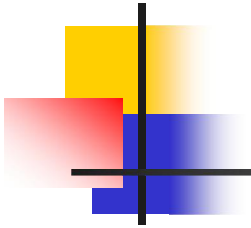
$$R_{on} = \left(1/R_N + 1/R_P \right)^{-1}$$

对称设计时 $R_{on} = \dfrac{1}{2K(V_{DD} - 2V_T)}$

CMOS传输门：RC延迟



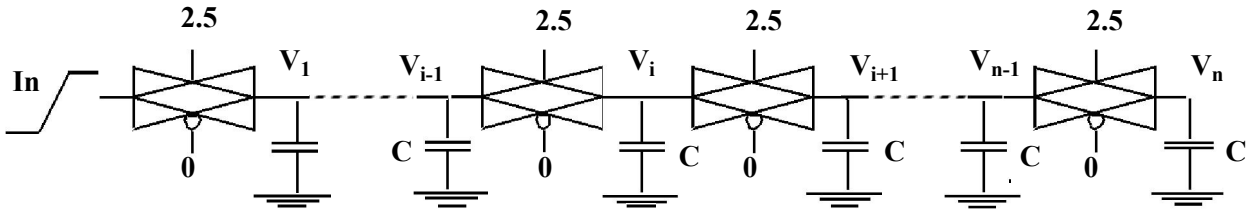
- 利用高效电阻为低效电阻一半的结论
- 对称设计：**Kn＝Kp＝2K0，Wp＝2Wn＝2W，Rn＝Rp＝R0/2**
- 如果负载电容只有传输管的漏电容，则传输延迟：$t_{pHL} = t_{pLH} \propto R_0 C_0$
- 相同尺寸：**Wp＝Wn＝W，Kn＝2Kp＝2K，Rn＝Rp/2＝R0/2**，则传输延迟：$t_{pLH} \propto R_0 C_0$　$t_{pHL} \propto 0.8 R_0 C_0$
- **CMOS传输门NP器件宽度相同为最优**



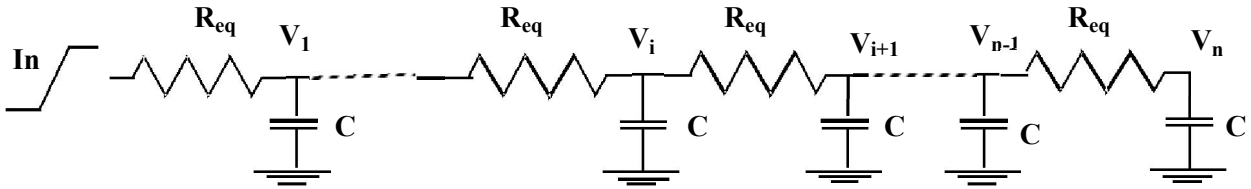
MOS传输门逻辑电路

- **NMOS/PMOS传输门特性**
- **CMOS传输门特性**
- 传输门的级联
- **NMOS传输门的电平恢复**

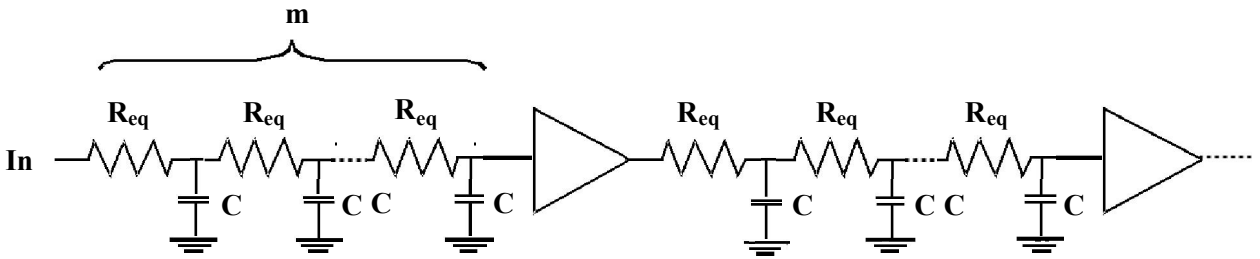
传输门的级联：RC网络



(a)

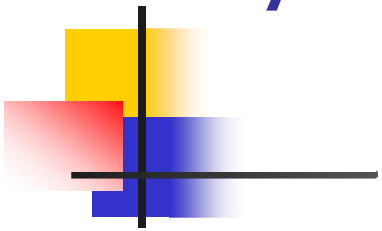


(b)



(c)

Delay Optimization



- **Delay of RC chain**

$$t_p = 0.69 \sum_{k=0}^{n} CR_{eq} k = 0.69 CR_{eq} \frac{n(n+1)}{2}$$

平方增加

- **Delay of Buffered Chain**

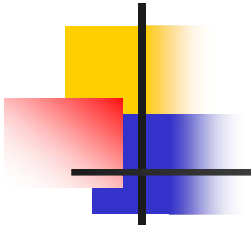
$$t_p = 0.69 \left\lfloor \frac{n}{m} CR_{eq} \frac{m(m+1)}{2} \right\rfloor + \left(\frac{n}{m} - 1 \right) t_{buf}$$

$$= 0.69 \left[CR_{eq} \frac{n(m+1)}{2} \right] + \left(\frac{n}{m} - 1 \right) t_{buf}$$

线性增加

$$m_{opt} = 1.7 \sqrt{\frac{t_{pbuf}}{CR_{eq}}}$$

传输门级联最多**3—4**个，再多则需要插入缓冲器



MOS传输门逻辑电路

- NMOS/PMOS传输门特性
- CMOS传输门特性
- 传输门的级联
- NMOS传输门的电平恢复

NMOS传输高电平：阈值损失

In

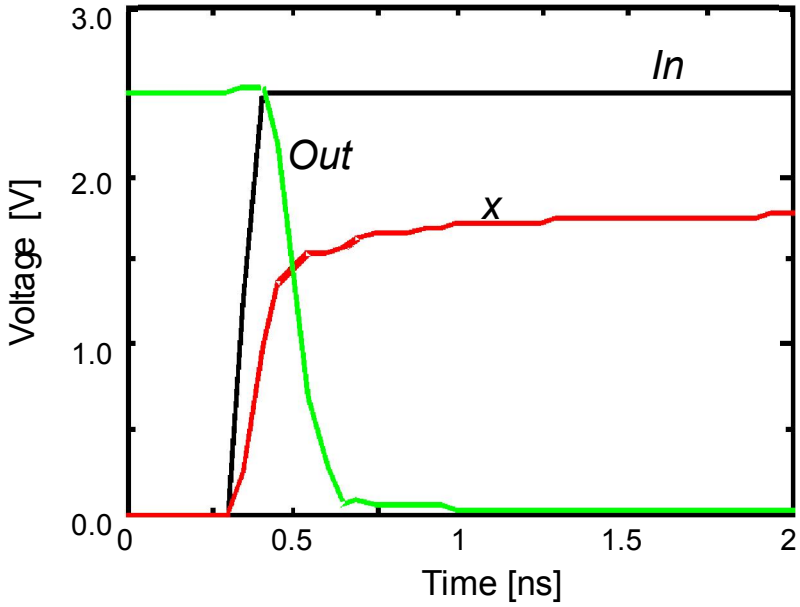
1.5μm/0.25μm

V_{DD} *x*

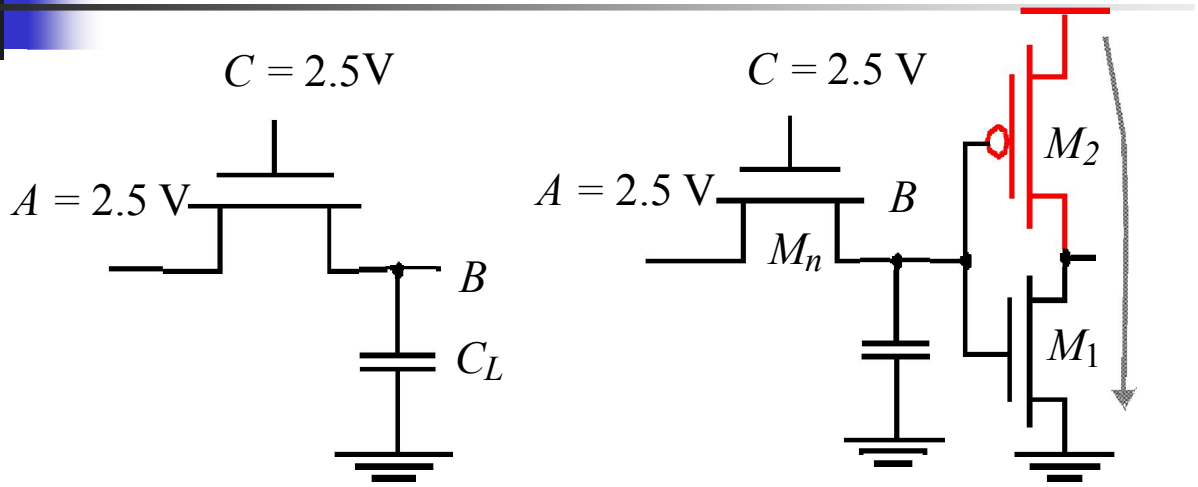
Out

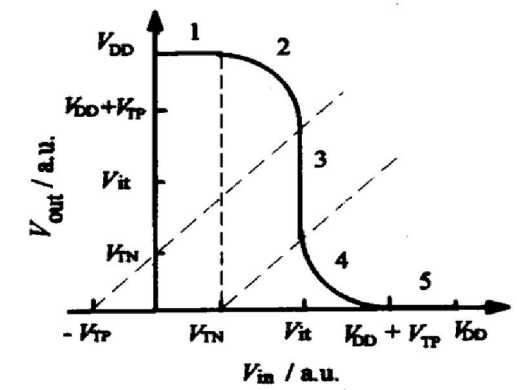
0.5μm/0.25μm

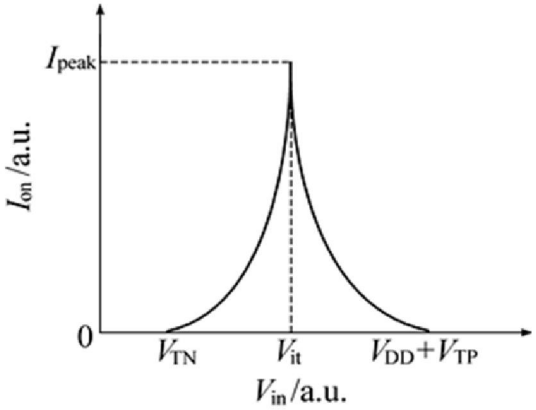
0.5μm/0.25μm



NMOS传输门







V_B does not pull up to 2.5V, but 2.5V - V_{TN}

- 阈值损失降低了噪声容限，并引起静态短路功耗
- 可以采用**CMOS**传输门，但是结构复杂

NMOS 传输门: 电平恢复器件

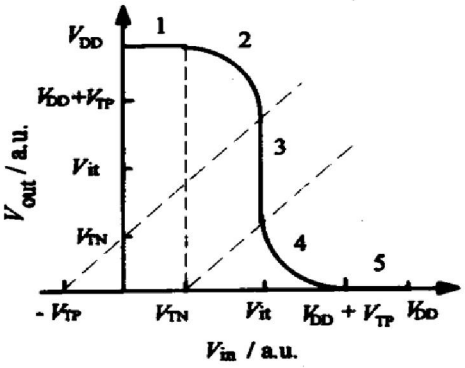
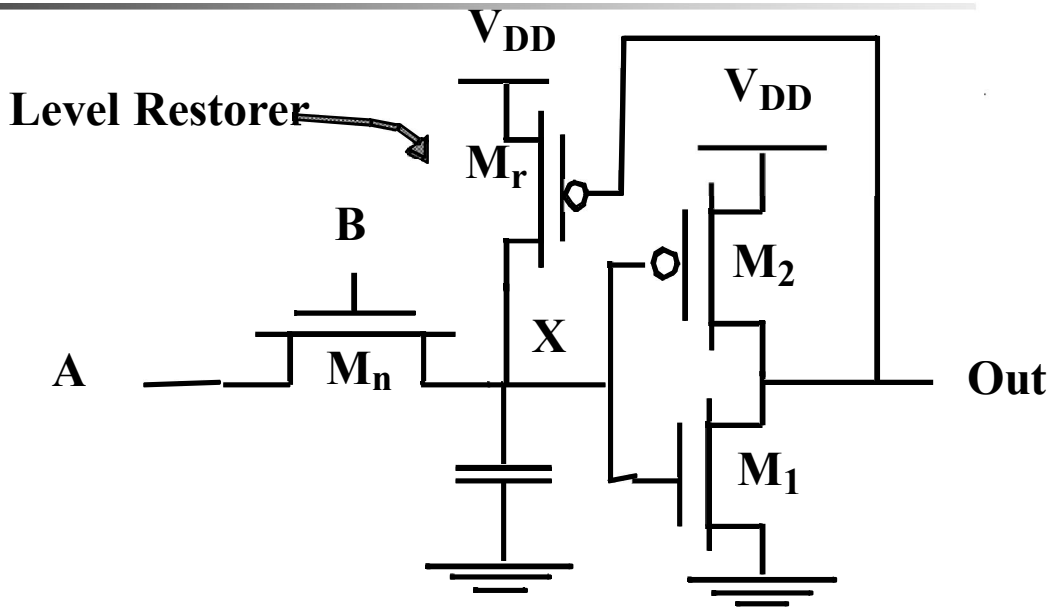
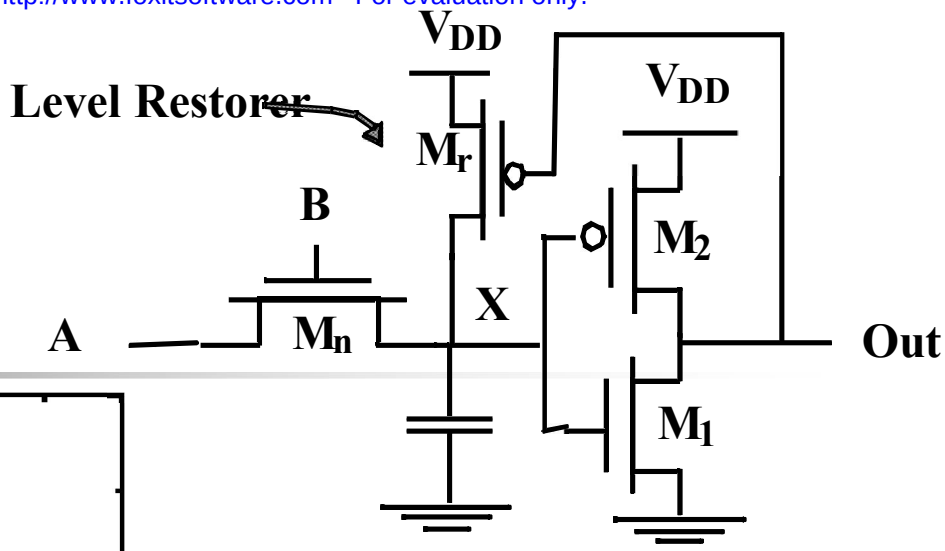


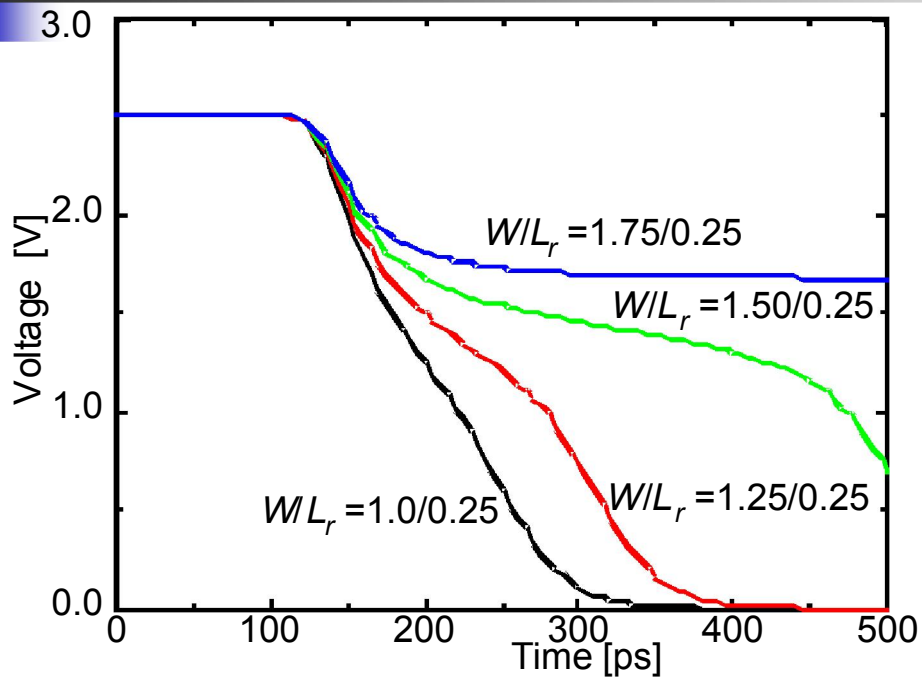
图 4.1.4 理想 CMOS 反相器的直流电压传输特性曲线



- 优点：输出信号全摆幅
- 缺点：增加了X和out节点电容，X节点放电过程Mr和Mn竞争
- 折中方案：限制Mr电流

Restorer Sizing





- 电平恢复作用的PMOS器件Mr的宽长比不能太大，否则电路无法工作
- Mr一般取最小尺寸L×L，这样引入漏区电容最小
- 如果前级NMOS传输门串联级数较多，Mr甚至可以取为倒比例（W/L<1）