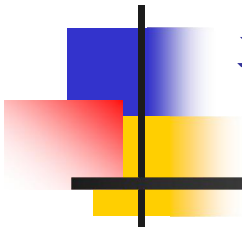
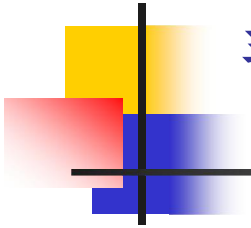


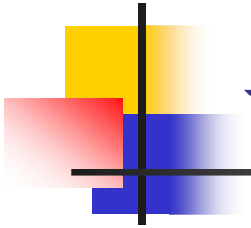
静态CMOS逻辑电路

4.4 与非门/或非门



静态CMOS逻辑电路

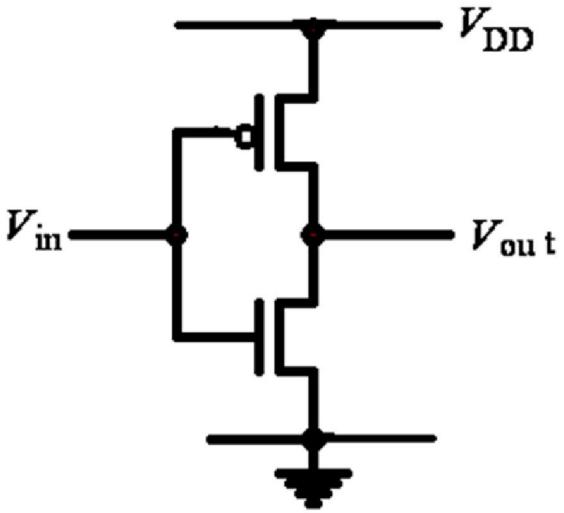
- **4.4** 与非门/或非门
- **4.5** 复杂逻辑门的设计
- **4.6 CMOS**逻辑电路的功耗

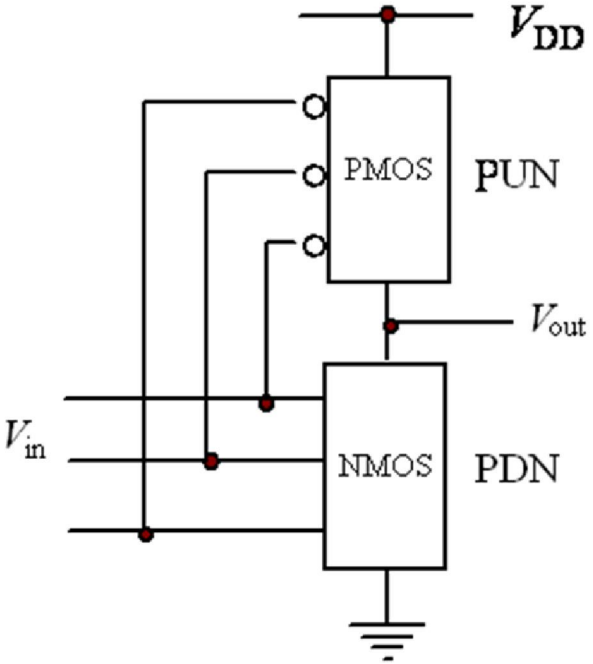


与非门/或非门

- 与非门的直流特性
- 与非门的瞬态特性
- 与非门的设计
- 或非门

从反相器到逻辑门的构成

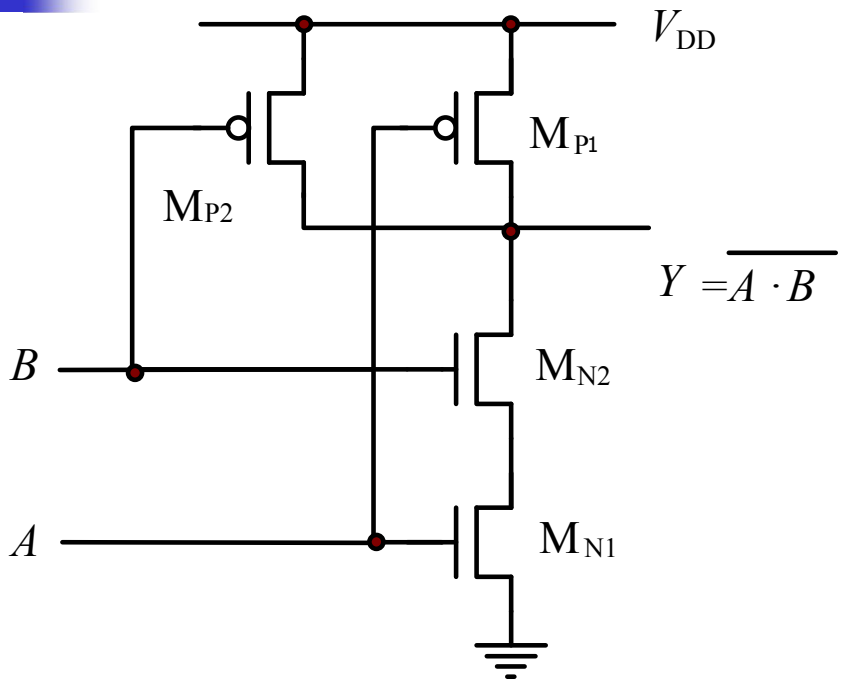




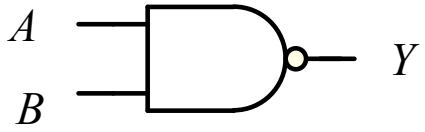
把单个**PMOS**管和**NMOS**管
换成多个串、并联的管子

CMOS与非门

电路图



逻辑符号与真值表



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

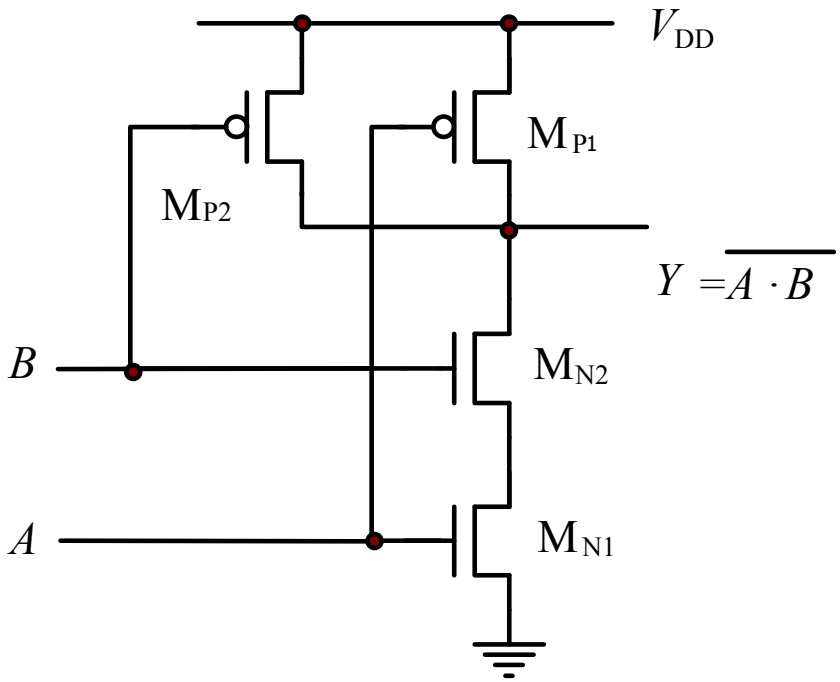
CMOS二输入与非门

一、直流电压传输特性

使用等效反相器方法分析

分两种情况：

1. 两个输入信号同步
2. 两个输入信号不同步

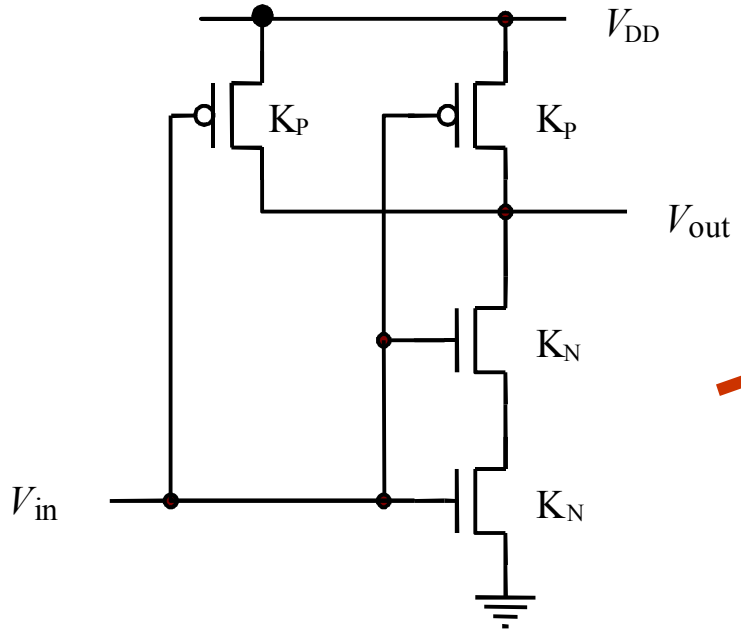


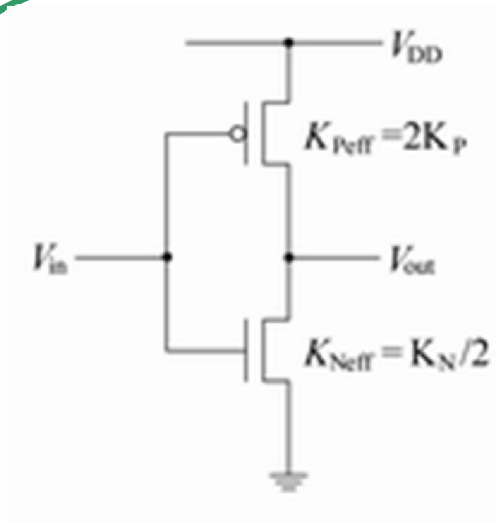
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

注意： 对不同输入状态，等效反相器参数不同。

直流电压传输特性—两个输入信号同步

如果两个输入信号同步





$$K_{Neff} = \frac{K_{N1} \bullet K_{N2}}{K_{N1} + K_{N2}}$$

$$K_{Peff} = K_{P1} + K_{P2}$$

两输入同步情况下逻辑阈值电平

$$V_{it}=\frac{V_{TN}+\sqrt{1/K\text{reff}}\,(V_{DD}+V_{TP})}{1+\sqrt{1/K\text{reff}}},\quad K_{\text{reff}}=K_{\text{Neff}}\Big/K_{\text{Peff}}=K_N/4K_P$$

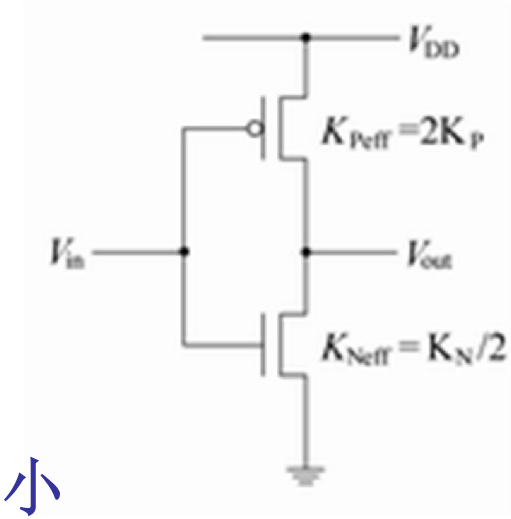
$$V_{it}=\frac{V_{TN}+2\sqrt{1/Kr}\,(V_{DD}+V_{TP})}{1+2\sqrt{1/Kr}}$$

$$K_r=K_N/K_P$$

若$K_N=K_P,\ V_{TN}=-V_{TP},$

$$V_{it}=\frac{2V_{DD}-V_{TN}}{3}$$

高电平噪声容限变小



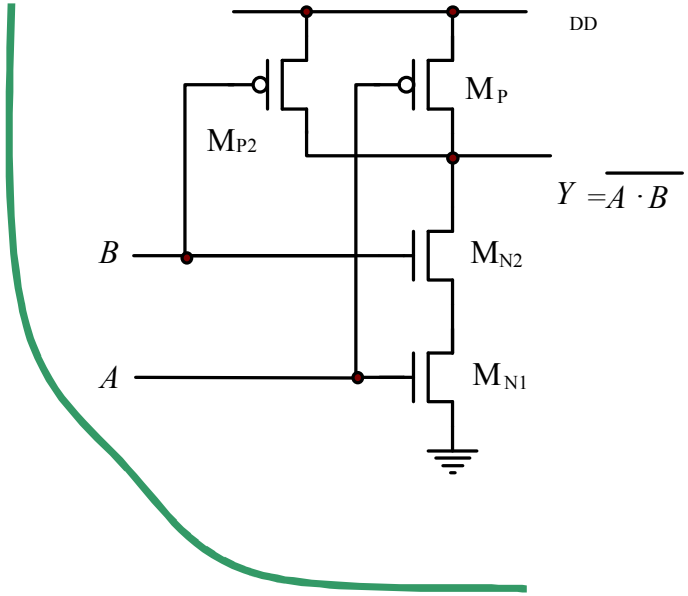
若要求最大的噪声容限 $V_{it}=\frac{1}{2}V_{DD}$，则$K_N/K_P=4$

直流电压传输特性— 两个输入信号不同步

特性条件

B固定在V_{DD}，输出随A变化的关系

A固定在V_{DD}，输出随B变化的关系



等效反相器

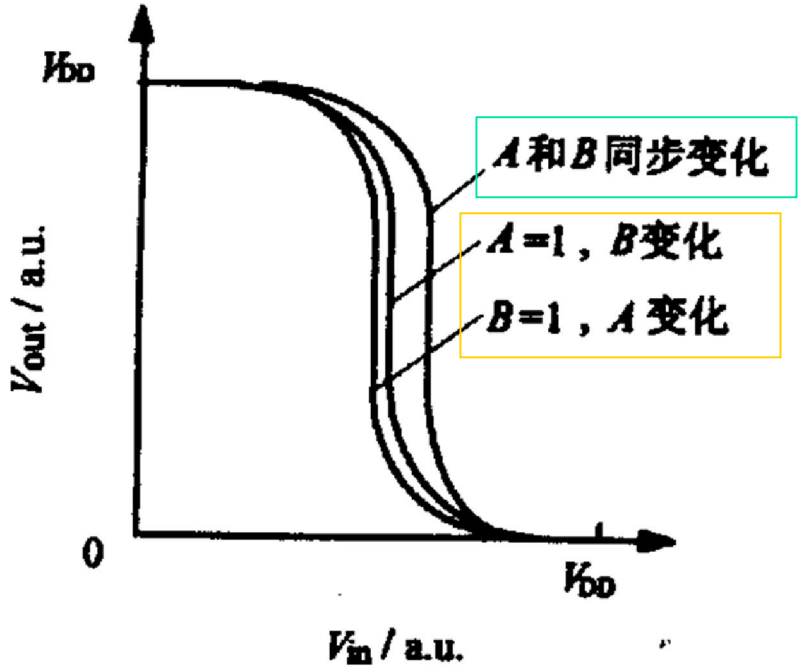
$$K_{\mathrm{Peff}} = K_{\mathrm{P}}, \quad K_{\mathrm{Neff}} \approx K_{\mathrm{N}}/2$$

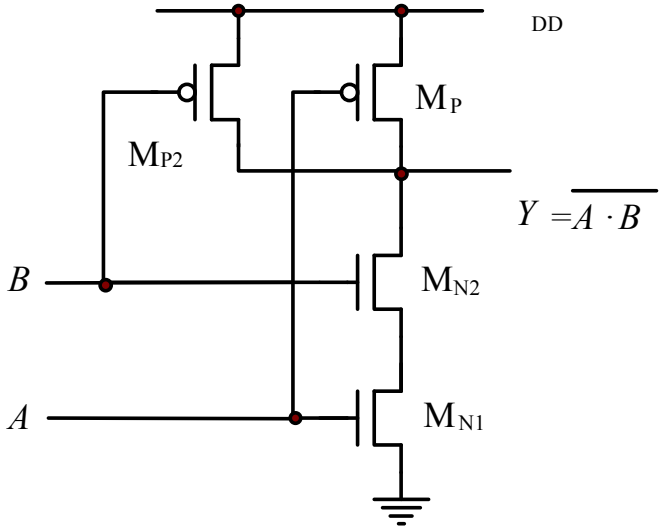
$$K_{reff} = K_{Neff} / K_{Peff} = K_r / 2$$

等效反相器阈值 $$V_{it} = \frac{V_{\mathrm{TN}} + \sqrt{2/K_{\mathrm{r}}}(V_{\mathrm{DD}} + V_{\mathrm{TP}})}{1 + \sqrt{2/K_{\mathrm{r}}}}$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

二输入与非门的直流电压传输特性曲线





Issue:
A变化和B变化的差别

等效反相器阈值 $V_{it} = \dfrac{V_{TN} + \sqrt{2/K_r}(V_{DD} + V_{TP})}{1 + \sqrt{2/K_r}}$

$V_{it} = \dfrac{V_{TN} + 2\sqrt{1/K_r}(V_{DD} + V_{TP})}{1 + 2\sqrt{1/K_r}}$

分析n输入与非门的直流特性

n个输入信号同步时的逻辑阈值

$$V_{\mathrm{n}}=\frac{V_{\mathrm{TN}}+n\sqrt{1/K_{\mathrm{r}}}\left(V_{\mathrm{DD}}+V_{\mathrm{TP}}\right)}{1+n\sqrt{1/K_{\mathrm{r}}}}$$

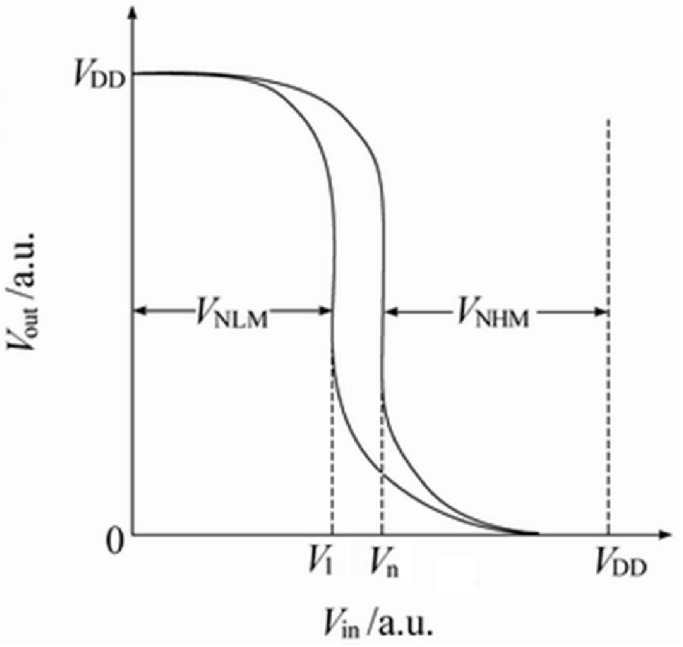
n个输入信号不同步时

忽略衬偏效应，有（n－1）种情况

n个输入信号只有1个输入变化，

其余固定在高电平的逻辑阈值

$$V_{1}=\frac{V_{\mathrm{TN}}+\sqrt{n/K_{\mathrm{r}}}\left(V_{\mathrm{DD}}+V_{\mathrm{TP}}\right)}{1+\sqrt{n/K_{\mathrm{r}}}}$$

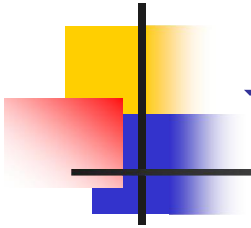


最佳直流特性

$$V_{\mathrm{NLM}}=V_{\mathrm{NHM}}$$

$$V_{\mathrm{NLM}}=V_{1},\quad V_{\mathrm{NHM}}=V_{\mathrm{DD}}-V_{\mathrm{n}}$$

$$K_{\mathrm{N}}/K_{\mathrm{P}}=n^{3/2}$$



与非门/或非门

- 与非门的直流特性
- 与非门的瞬态特性
- 与非门的设计
- 或非门

二 与非门瞬态特性

使用等效反相器方法分析

1. 上升时间

$$t_r = \tau_r \left[\frac{\alpha_P - 0.1}{(1-\alpha_P)^2} + \frac{1}{2(1-\alpha_P)} \ln\left(\frac{1.9-2\alpha_P}{0.1}\right) \right]$$

$$\tau_r = \frac{C_L}{K_{Peff} V_{DD}}$$

最坏情况 $K_{Peff}=K_P$

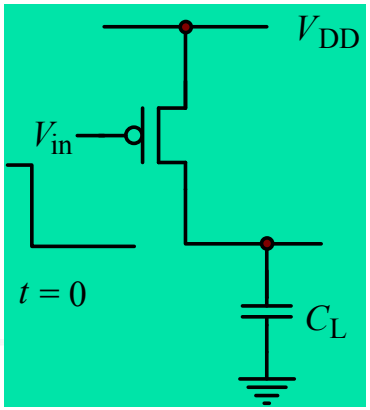
2. 下降时间

$$t_f = \tau_f \left[\frac{\alpha_N - 0.1}{(1-\alpha_N)^2} + \frac{1}{2(1-\alpha_N)} \ln\left(\frac{1.9-2\alpha_N}{0.1}\right) \right]$$

$$\tau_f = \frac{C_L}{K_{Neff} V_{DD}}$$

$K_{Neff}=K_N/n$

传输延迟时间：阶跃输入



- 输入信号变化到输出信号变化**50**%的时间

$$t_1 = \frac{\tau_r(\alpha_P - u_1)}{(1-\alpha_P)^2} \qquad t_2 = \frac{\tau_r}{2(1-\alpha_P)} \ln\left(\frac{1+u_2-2\alpha_P}{1-u_2}\right)$$

取：$t_r = t_1(u_1 = 0) + t_2(u_2 = 0.5)$

$$t_{pLH} = \frac{C_L}{K_{peff}(V_{DD}-|V_{TP}|)}\left[\frac{|V_{TP}|}{V_{DD}-|V_{TP}|} + \frac{1}{2}\ln\left(\frac{4(V_{DD}-|V_{TP}|)}{V_{DD}} - 1\right)\right]$$

$$= \tau_r\left[\frac{\alpha_P}{(1-\alpha_P)^2} + \frac{1}{2(1-\alpha_P)}\ln(3-4\alpha_P)\right]$$

传输延迟：非阶跃输入近似

- 等效反相器
- 用**PMOS**和**NMOS**的等效导电因子

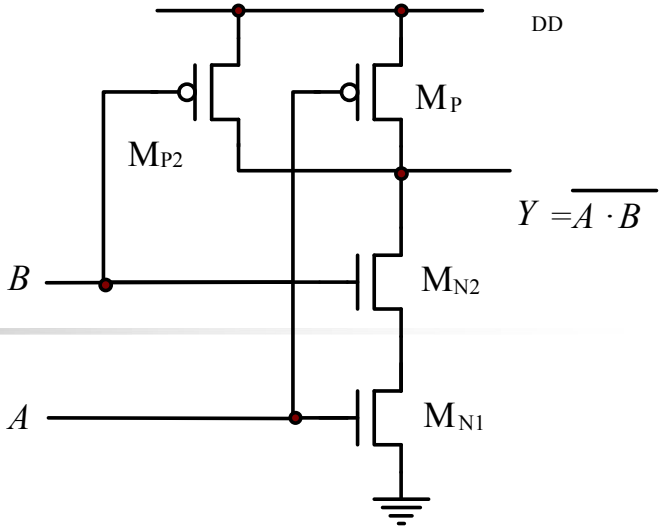
$$t_{\mathrm{p}} = \frac{t_{\mathrm{pHL}} + t_{\mathrm{pLH}}}{2}$$

$$t_{\mathrm{pHL}} = \frac{C_{\mathrm{L}}\Delta V_{\mathrm{HL}}}{I_{\mathrm{av,HL}}} \approx \tau_{\mathrm{f}} \frac{1}{\left(1-\alpha_{\mathrm{N}}\right)^2}$$

$$t_{\mathrm{pLH}} = \frac{C_{\mathrm{L}}\Delta V_{\mathrm{LH}}}{I_{\mathrm{av,LH}}} \approx \tau_{\mathrm{r}} \frac{1}{\left(1-\alpha_{\mathrm{P}}\right)^2}$$

$$t_{\mathrm{p}} = \frac{1}{2}\tau_{\mathrm{r}}\left[\frac{1}{K_{\mathrm{r}}\left(1-\alpha_{\mathrm{N}}\right)^2} + \frac{1}{\left(1-\alpha_{\mathrm{P}}\right)^2}\right]$$

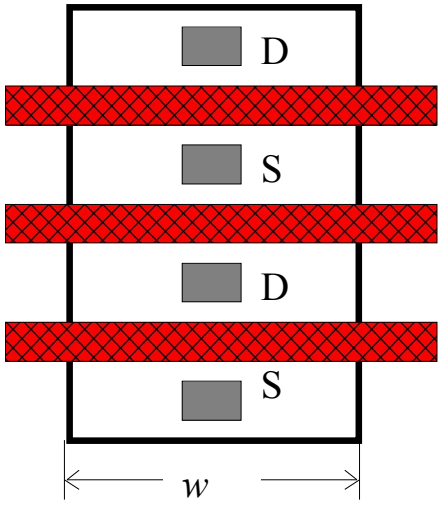
与非门瞬态特性:电容

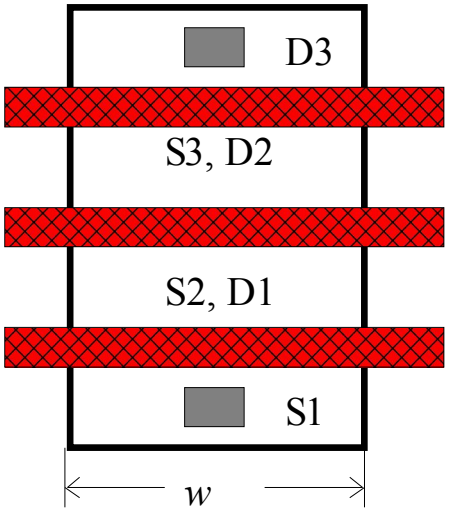


负载电容计算

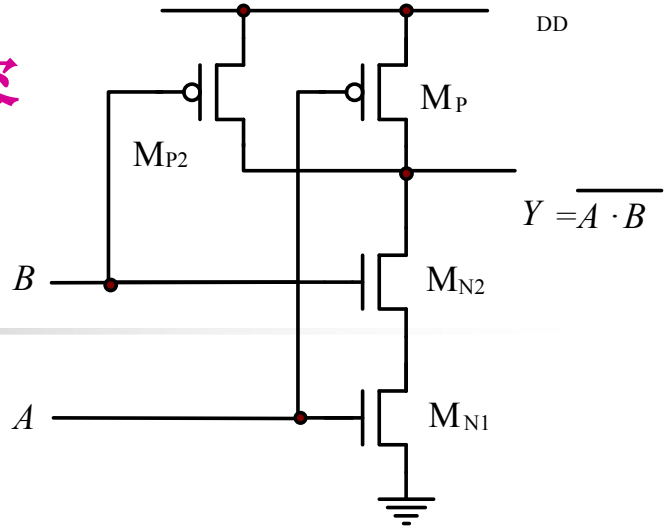
$$C_L = C_{DBN} + nC_{DBP} + C_{in} + C_l$$

MOS管串并联的影响

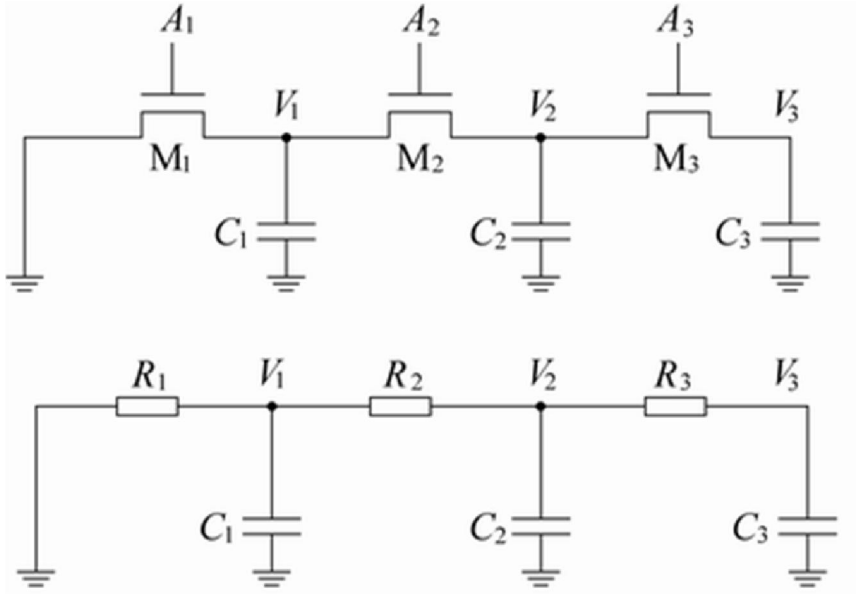




与非门瞬态特性：中间节点电容



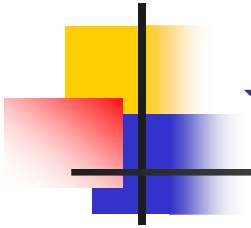
考虑中间节点电容放电



$$V_n(t) = V_{DD} e^{-t/\tau}$$

$$\tau = \sum_{i=1}^{n} \left(\sum_{j=1}^{i} R_j \right) C_i$$

Elmore模型，也可以根据不同要求采用集总模型



与非门/或非门

- 与非门的直流特性
- 与非门的瞬态特性
- 与非门的设计
- 或非门

与非门设计考虑

根据直流特性设计

$$V_{\mathrm{NLM}} = V_{\mathrm{NHM}}$$

$$V_1 + V_n = V_{\mathrm{DD}}$$

$$\Rightarrow K_{\mathrm{r}} = K_N / K_P = n^{3/2}$$

根据瞬态特性设计

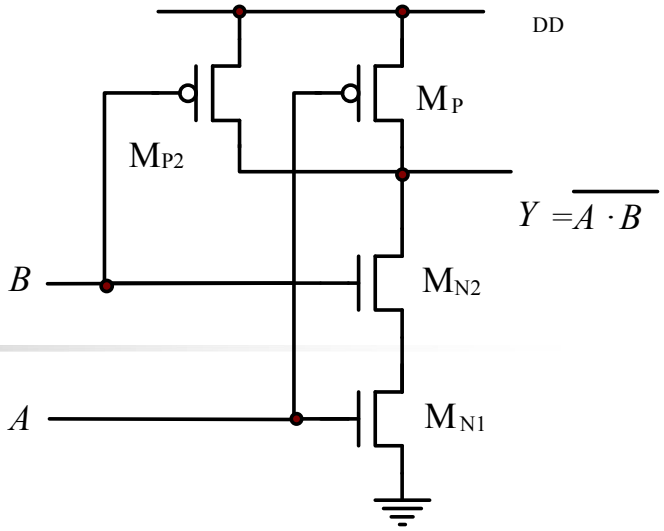
$$\tau_{\mathrm{r}} = \tau_{\mathrm{f}}$$

$$\Rightarrow K_{\mathrm{Neff}} = K_{\mathrm{Peff}}$$

对称与非门

$$\Rightarrow K_{\mathrm{r}} = K_{\mathrm{N}} / K_{\mathrm{P}} = n$$

对称与非门的瞬态特性：RC近似



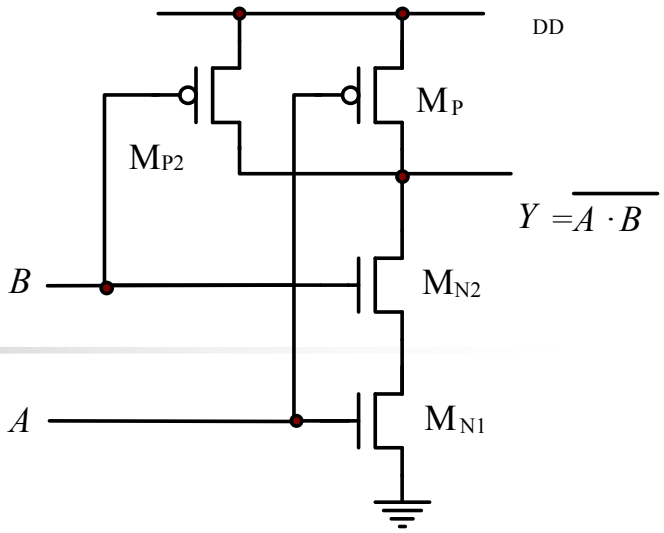
$$K_{\mathrm{Neff}} = K_{\mathrm{Peff}}$$

对称与非门

$$\Rightarrow K_{\mathrm{r}} = K_{\mathrm{N}} / K_{\mathrm{P}} = n$$

- 设电子迁移率为空穴2倍，器件阈值相等，工艺允许最小沟道宽度为W_0，宽度为W_0的PMOS导电因子为K_0，沟道等效电阻为R_0，源漏区电容为C_0
- 对称与非门：$W_N = \frac{n}{2} W_P = \frac{nW_0}{2}$
- 则NMOS串联等效电阻也为R_0

对称与非门的瞬态特性：RC近似



$$W_N = \frac{n}{2} W_P = \frac{nW_0}{2}$$

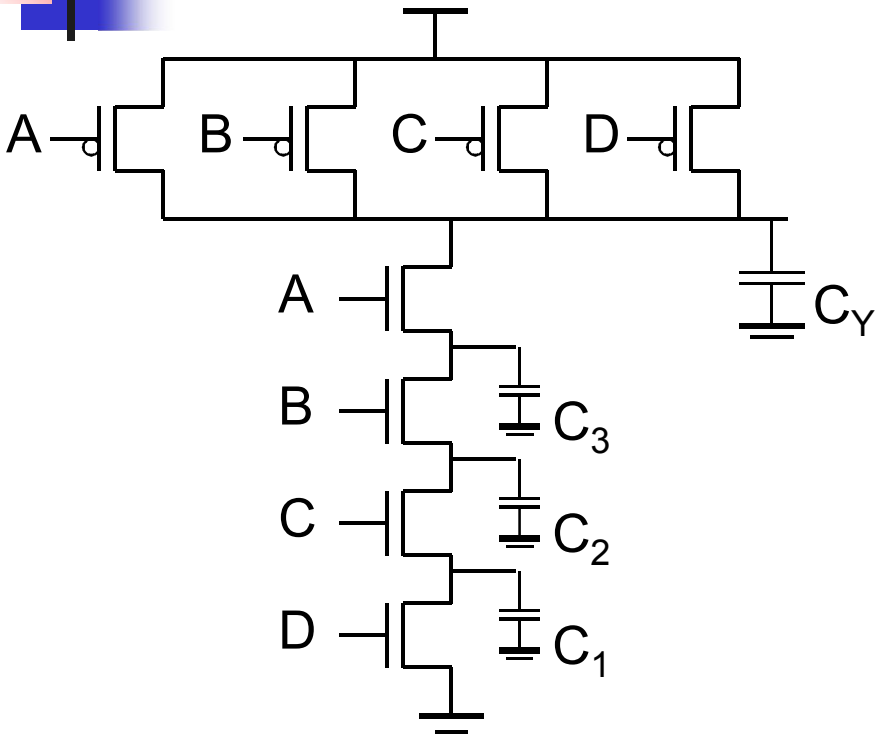
- 没有负载情况，对串联NMOS利用RC集总模型，则Y点的总电容

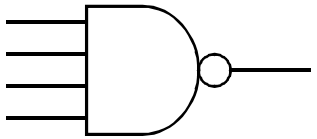
$$C_Y = nC_0 + n\frac{n}{2}C_0 = n(\frac{n}{2}+1)C_0$$

- 如果忽略NMOS串联网络的中间节点电容

$$C_Y = nC_0 + \frac{n}{2}C_0 = \frac{3n}{2}C_0$$

Fan-In：扇入

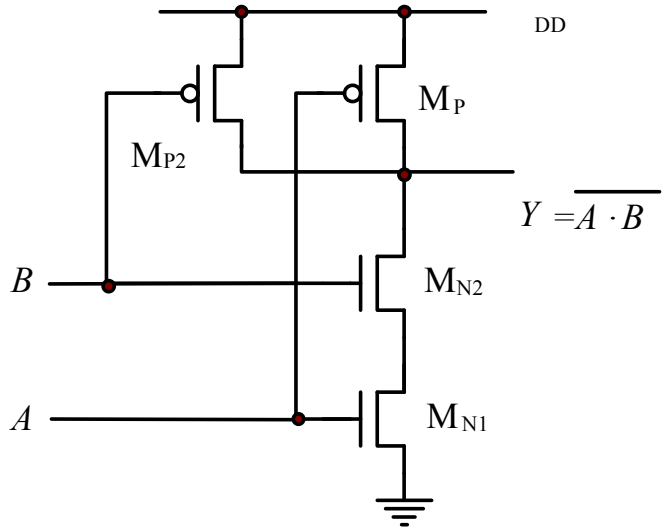




$$C_Y = nC_0 + n\frac{n}{2}C_0 = n(\frac{n}{2}+1)C_0$$

对称与非门：上升延迟时间

- 最大上升延迟为单个PMOS上拉
- 则上升延迟时间同扇入的数目呈线性关系



$$t_{pLH} \propto \frac{3n}{2} R_0 C_0$$

$$W_N = \frac{n}{2} W_P = \frac{nW}{2}$$

Rp=R0

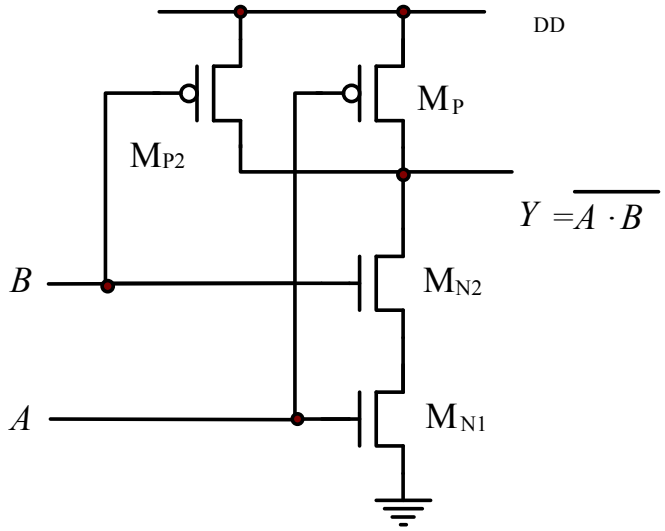
$$C_L = nC_0 + \frac{n}{2} C_0 = \frac{3n}{2} C_0$$

对称与非门：下降延迟时间

- 下降延迟为串联NMOS下拉
- 则下降延迟时间同扇入的数目呈平方关系

$$t_{pHL} \propto \frac{n^2 + 2n}{2} R_0 C_0$$

- 当n较大时，对称与非门的上升和下降延迟差别较多
- 对称与非门只是等效导电因子相等



$$W_N = \frac{n}{2} W_P = \frac{nW}{2}$$

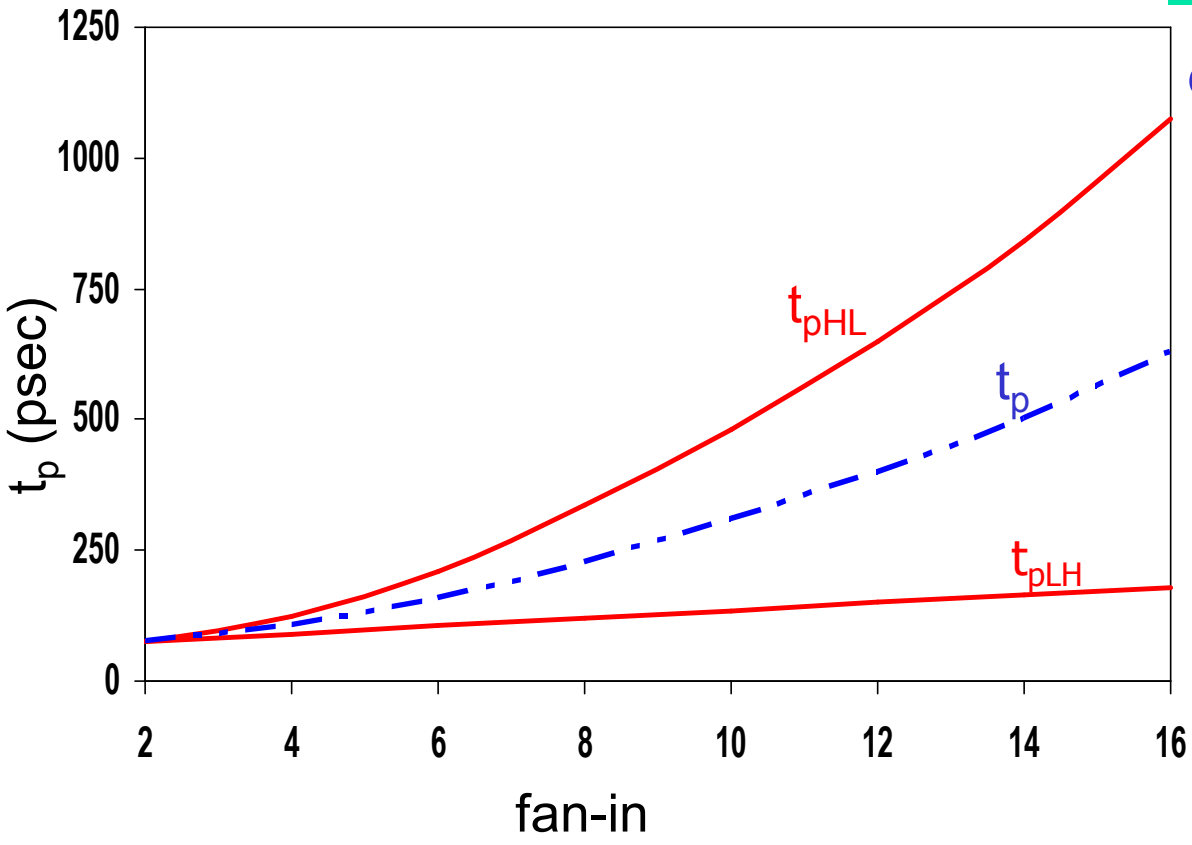
Rn＝R0

$$C_L = n(\frac{n}{2} + 1) C_0$$

t_p as a Function of Fan-In

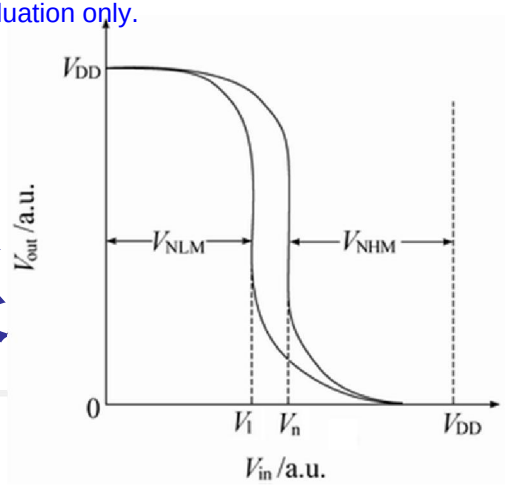
$$t_{pHL} \propto \frac{n^2 + 2n}{2} R_0 C_0$$

$$t_{pLH} \propto \frac{3n}{2} R_0 C_0$$



数字逻辑门
的扇入数目
一般不大于4

对称与非门：噪声容限



$$V_n = \frac{V_{TN} + n\sqrt{1/K_r}\,(V_{DD} + V_{TP})}{1 + n\sqrt{1/K_r}}$$

$$V_l = \frac{V_{TN} + \sqrt{n/K_r}\,(V_{DD} + V_{TP})}{1 + \sqrt{n/K_r}}$$

对称与非门

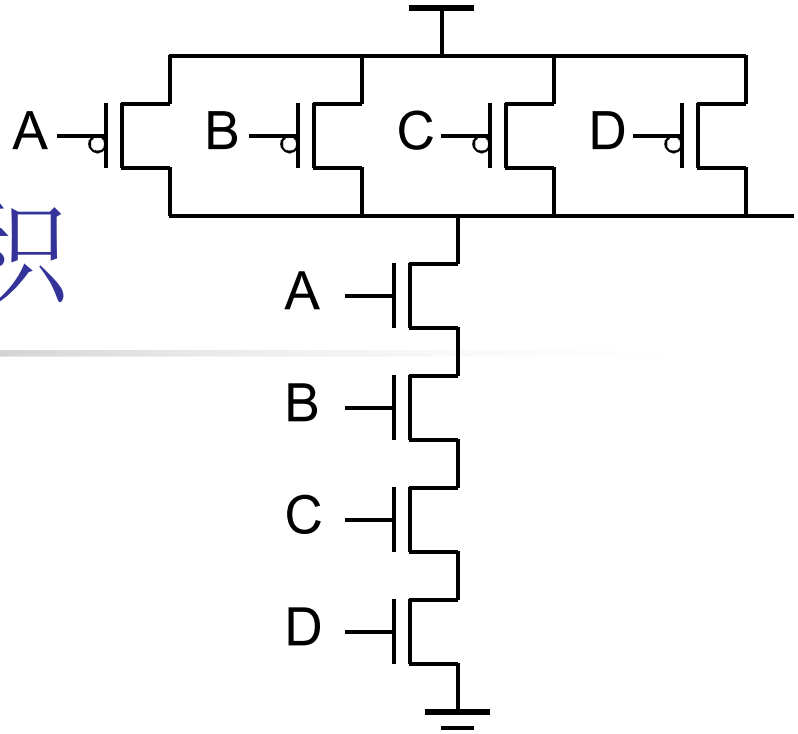
$$K_{Neff} = K_{Peff}$$

$$\Rightarrow K_r = K_N / K_P = n$$

- 则低电平噪声容限V_{NLM}＝VDD/2，高电平噪声容限：

$$V_{NHM} = V_{DD} - \frac{V_{TN} + \sqrt{n}\,(V_{DD} + V_{TP})}{1 + \sqrt{n}}$$

对称与非门：面积



- 用电路中所有器件的宽度之和间接表示面积

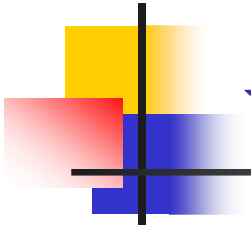
- **W0为PMOS的宽度，则N输入对称与非门的面积随着扇入的数目平方增加**

$$\Rightarrow K_{\text{Neff}} = K_{\text{Peff}}$$

$$\Rightarrow K_{\text{r}} = K_{\text{N}} / K_{\text{P}} = n$$

$$W_{total} = nW_0 + \frac{n^2}{2}W_0 = \frac{n^2 + 2n}{2}W_0$$

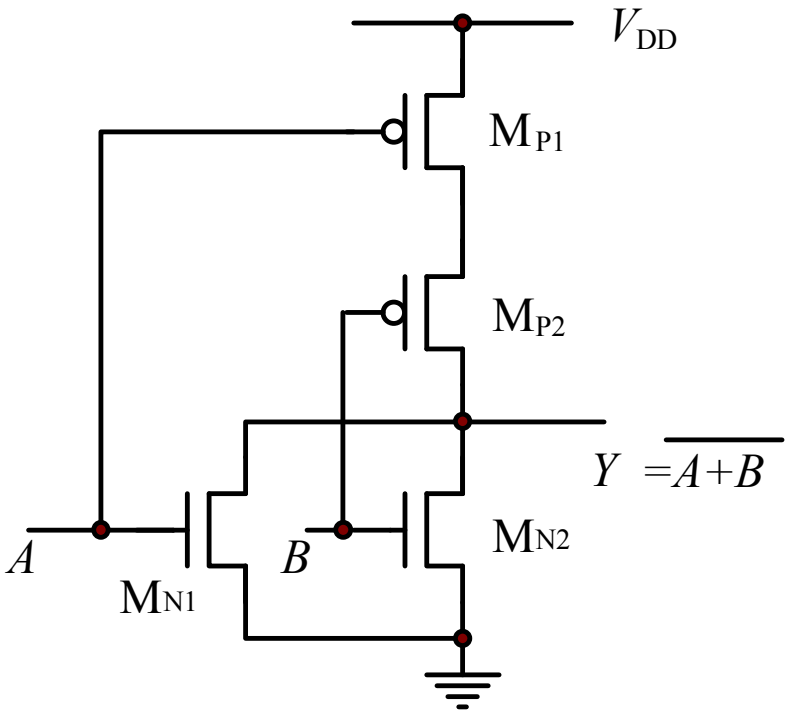
$$W_N = \frac{n}{2}W_P = \frac{nW_0}{2}$$



与非门/或非门

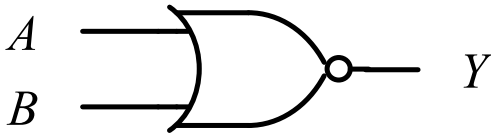
- 与非门的直流特性
- 与非门的瞬态特性
- 与非门的设计
- 或非门

CMOS或非门



电路图

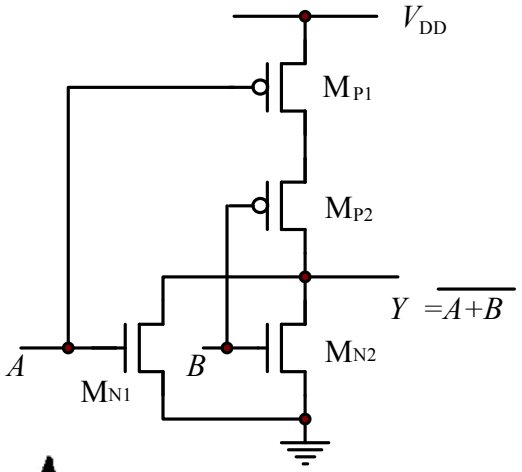
逻辑图

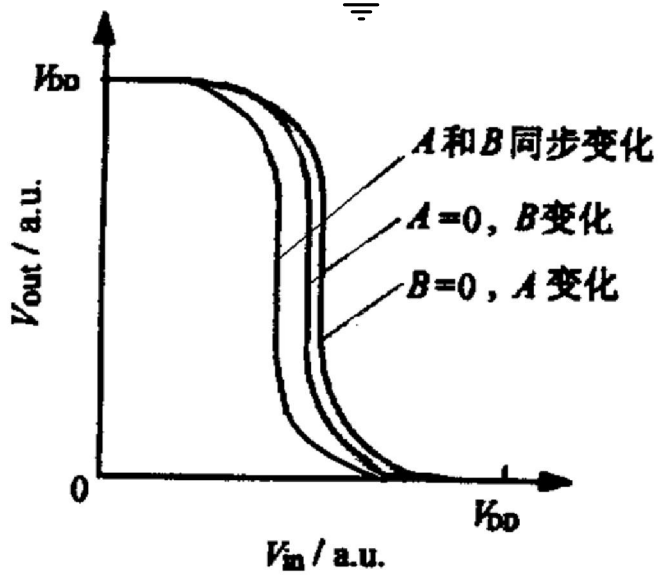


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

真值表

或非门的直流电压传输特性曲线





A和B同步变化

$$V_{it} = \frac{V_{TN} + \frac{1}{2}\sqrt{1/K_r}(V_{DD} + V_{TP})}{1 + \frac{1}{2}\sqrt{1/K_r}}$$

一个输入变化

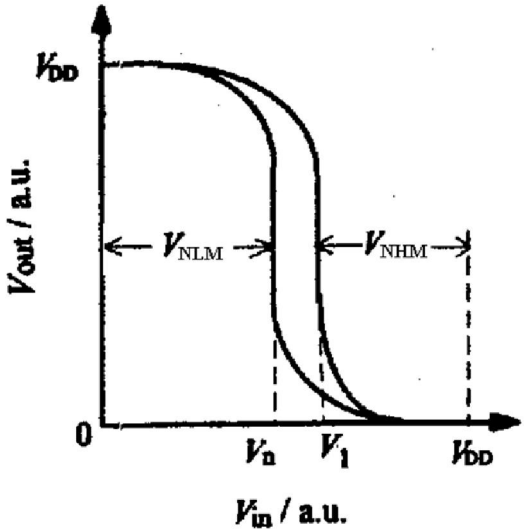
$$V_{it} = \frac{V_{TN} + \sqrt{1/2K_r}(V_{DD} + V_{TP})}{1 + \sqrt{1/2K_r}}$$

n输入或非门直流特性

n输入同步变化与1个输入变化的逻辑阈值

$$V_1 = \frac{V_{TN} + \sqrt{1/nK_r}(V_{DD} - V_{TP})}{1 + \sqrt{1/nK_r}}$$

$$V_n = \frac{V_{TN} + \frac{1}{n}\sqrt{1/K_r}(V_{DD} - V_{TP})}{1 + \frac{1}{n}\sqrt{1/K_r}}$$



考虑n输入同步变化与1个输入变化两种极端情况

$$V_{NLM} = V_n$$

$$V_{NHM} = V_{DD} - V_1$$

n输入或非门瞬态特性

1. 上升时间

$$t_r = \tau_r \left[\frac{\alpha_P - 0.1}{(1-\alpha_P)^2} + \frac{1}{2(1-\alpha_P)} \ln\left(\frac{1.9-2\alpha_P}{0.1} \right) \right]$$

$$\tau_r = \frac{C_L}{K_{Peff} V_{DD}}$$

2. 下降时间

$$t_f = \tau_f \left[\frac{\alpha_N - 0.1}{(1-\alpha_N)^2} + \frac{1}{2(1-\alpha_N)} \ln\left(\frac{1.9-2\alpha_N}{0.1} \right) \right]$$

$$\tau_f = \frac{C_L}{K_{Neff} V_{DD}}$$

注意： 上升时间要考虑中间节点电容充电

负载电容 $C_L = nC_{DBN} + C_{DBP} + C_{in} + C_l$

或非门设计考虑

根据直流特性设计

$$V_{\mathrm{NLM}} = V_{\mathrm{NHM}}$$

$$V_1 + V_n = V_{\mathrm{DD}}$$

$$\Rightarrow K_{\mathrm{r}} = K_N / K_P = n^{-3/2}$$

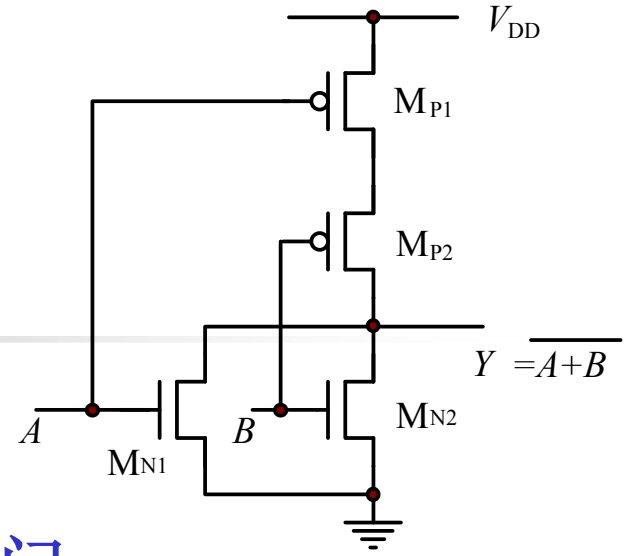
根据瞬态特性设计

$$\tau_r = \tau_f$$

$$\Rightarrow K_{\mathrm{Neff}} = K_{\mathrm{Peff}}$$

$$\Rightarrow K_{\mathrm{r}} = K_N / K_P = n^{-1}$$

对称或非门的瞬态特性：RC近似



$$\tau_r = \tau_f$$

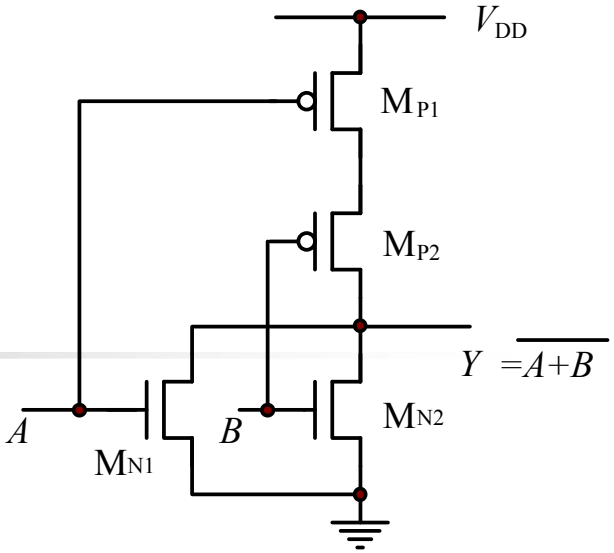
$$\Rightarrow K_{\text{Neff}} = K_{\text{Peff}}$$

$$\Rightarrow K_{\text{r}} = K_N / K_P = n^{-1}$$

对称或非门

- 电子迁移率为空穴2倍，器件阈值相等
- 对称或非门：取宽度Wp＝W0 的PMOS，定义其漏区电容为C0，等效电阻Rp＝R0
- 则器件宽度应为 $W_N = \frac{W_0}{2}, W_P = nW_0$ 等效电阻均为为R0

对称或非门的瞬态特性：RC近似



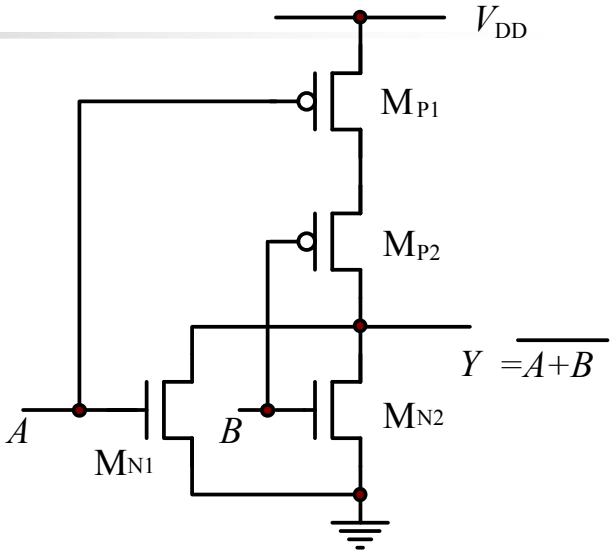
$$W_N = \frac{W_0}{2}, W_P = nW_0$$

- 没有负载情况，串联PMOS利用RC集总模型，则Y点的电容

$$C_Y = \frac{n}{2}C_0 + n * nC_0 = n(n + \frac{1}{2})C_0$$

对称或非门：上升延迟时间

- 上升延迟为PMOS串联上拉
- 则上升延迟时间同扇入的数目呈平方关系



$$t_{pLH} \propto (n^2 + \frac{n}{2}) R_0 C_0$$

$$W_N = \frac{W_0}{2}, W_P = nW_0$$

Rn=R0

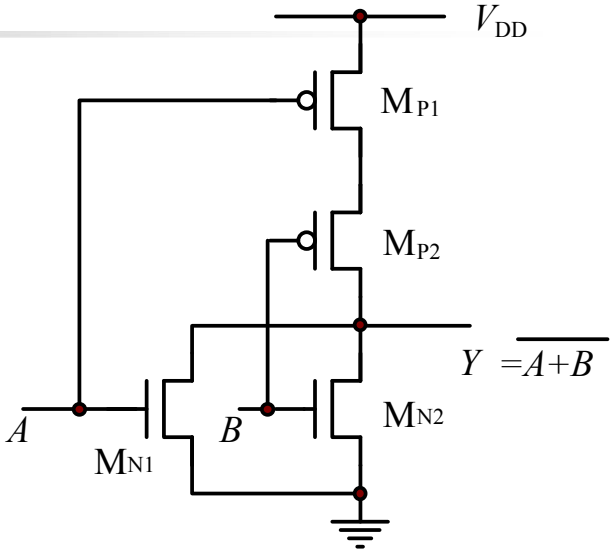
$$C_Y = n(n + \frac{1}{2}) C_0$$

对称或非门：下降延迟时间

- 下降延迟为单管NMOS下拉
- 则下降延迟时间同扇入的数目呈线性关系

$$t_{pHL} \propto \frac{3n}{2} R_0 C_0$$

- 当n较大时，对称或非门的上升和下降延迟差别很大
- 对称或非门只是等效导电因子相等



$$W_N = \frac{W_0}{2}, W_P = nW_0$$

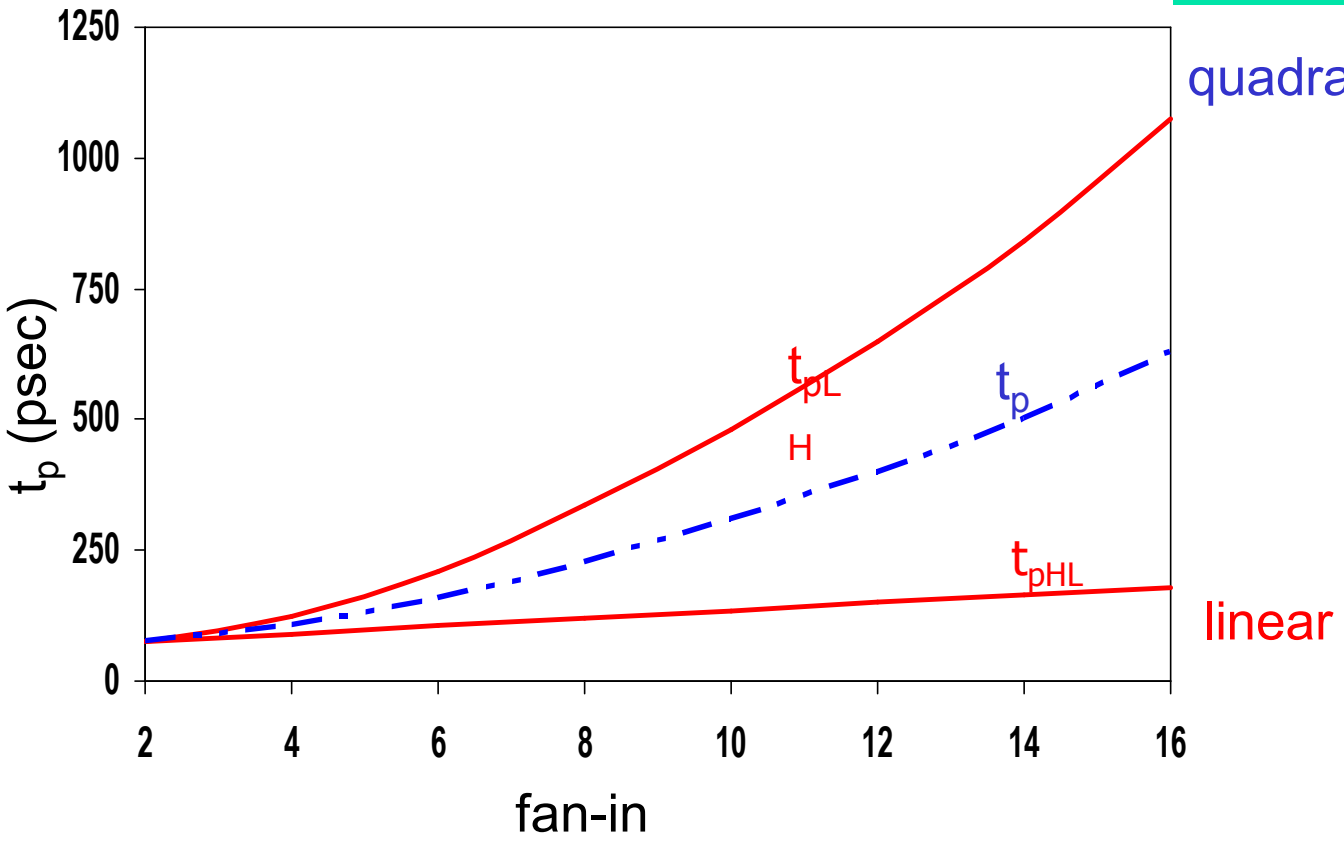
Rp＝R0

$$C_L = \frac{3}{2} nC_0$$

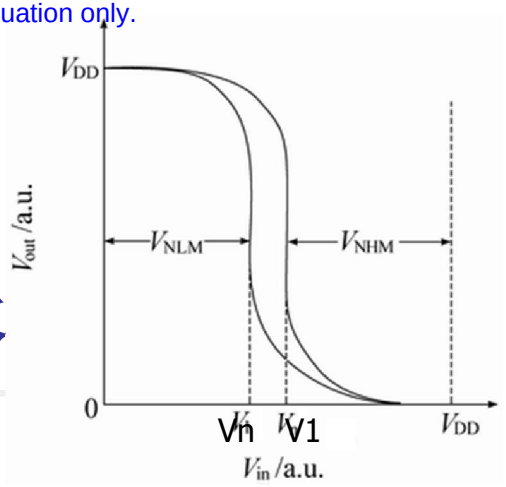
t_p as a Function of Fan-In

$$t_{pLH} \propto (n^2 + \frac{n}{2}) R_0 C_0$$

$$t_{pHL} \propto \frac{3n}{2} R_0 C_0$$



对称或非门：噪声容限



$$V_n = \frac{V_{TN} + \frac{1}{n}\sqrt{1/K_r}(V_{DD} + V_{TP})}{1 + \frac{1}{n}\sqrt{1/K_r}}$$

$$V_1 = \frac{V_{TN} + \sqrt{1/nK_r}(V_{DD} + V_{TP})}{1 + \sqrt{1/nK_r}}$$

对称或非门

$$\tau_r = \tau_f$$

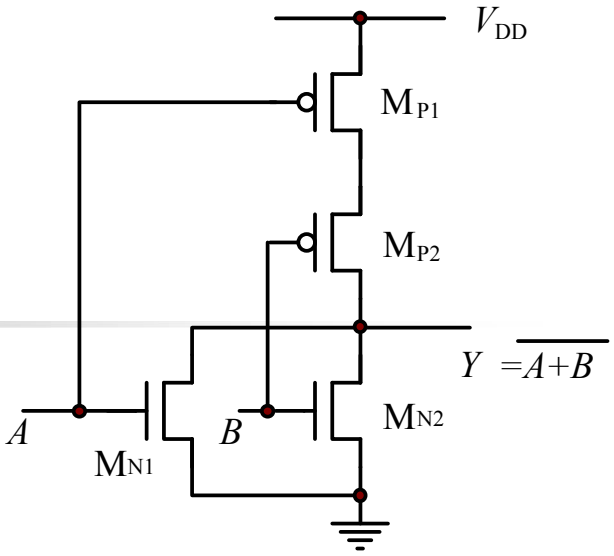
$$\Rightarrow K_{\mathrm{Neff}} = K_{\mathrm{Peff}}$$

$$\Rightarrow K_{\mathrm{r}} = K_N / K_P = n^{-1}$$

- 则高电平噪声容限V_{NHM}=VDD/2，低电平噪声容限:

$$V_{NLM} = V_n = \frac{V_{TN} + \sqrt{1/n}(V_{DD} + V_{TP})}{1 + \sqrt{1/n}}$$

对称或非门：面积



- 用电路中所有器件的宽度之和间接表示面积
- **W**为单位宽度，则**N**输入对称或非门的面积随着扇入的数目平方增加

$$W_N = \frac{W_0}{2}, W_P = nW_0$$

$$W_{total} = \frac{nW_0}{2} + n^2 W_0 = \frac{2n^2 + n}{2} W_0$$

对称设计：与非门/或非门

- 与非门实现电路效率更高

对称与非门

$$W_N = \frac{n}{2} W_P = \frac{nW_0}{2}$$

$$t_{pHL} \propto \frac{n^2 + 2n}{2} R_0 C_0$$

$$t_{pLH} \propto \frac{3n}{2} R_0 C_0$$

$$W_{total} = \frac{n^2 + 2n}{2} W_0$$

对称或非门

$$W_N = \frac{W_0}{2}, W_P = nW_0$$

$$t_{pLH} \propto (n^2 + \frac{n}{2}) R_0 C_0$$

$$t_{pHL} \propto \frac{3n}{2} R_0 C_0$$

$$W_{total} = \frac{2n^2 + n}{2} W_0$$

或非门设计范例

采用**0.6**微米工艺，设计一个两输入或非门，

- 要求在最坏情况下输出上升时间和下降时间不大于**0.5ns**
- 已知：

$$C_L = 1\text{pF}, \quad V_{DD} = 5\text{V}, \quad V_{TN} = 0.8\text{V}, \quad V_{TP} = -0.9\text{V}$$

$$K_N' = 120\,\mu\text{A}/\text{V}^2, \quad K_p' = 60\,\mu\text{A}/\text{V}^2$$

采用等效反相器方法

根据 $$t_r = \frac{C_L}{K_{peff} V_{DD}} \left[\frac{\alpha_P - 0.1}{1-\alpha_P} + \frac{1}{2(1-\alpha_P)} \ln \frac{1.9 - 2\alpha_P}{0.1} \right]$$

可得到 $$K_{peff} = 7.4 \times 10^{-4} (\mathrm{A/V^2})$$

同理可得到 $$K_{Neff} = 6.90 \times 10^{-4} (\mathrm{A/V^2})$$

或非门中**2个PMOS管串联** $$K_{p1} = K_{p2} = 2K_{peff} = 14.8 \times 10^{-4} (\mathrm{A/V^2})$$

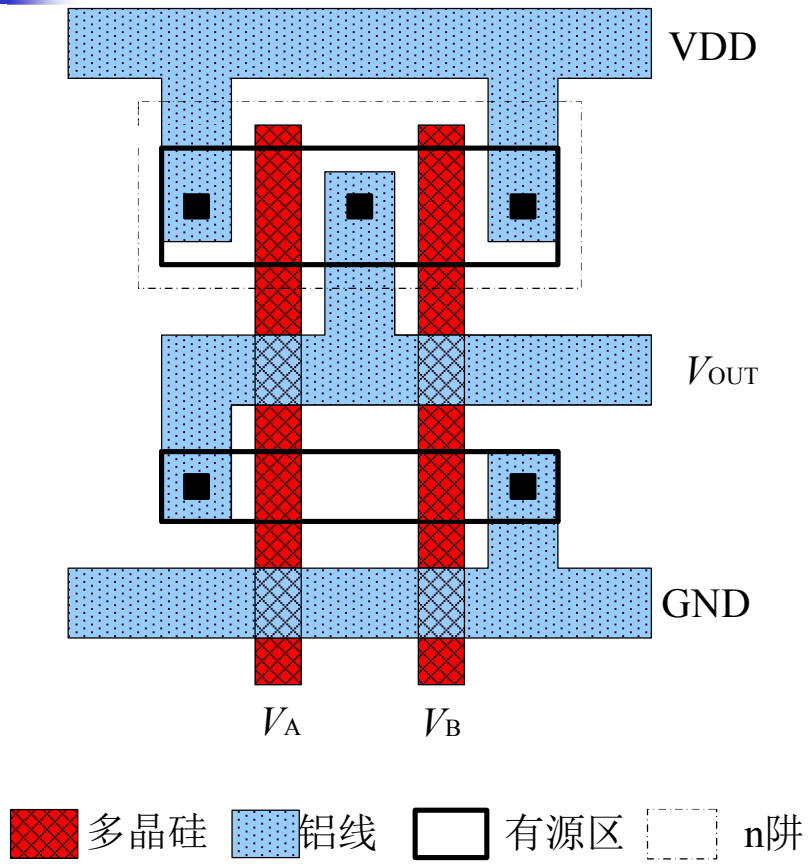
最坏情况下只有一个**NMOS管导通** $$K_{N1} = K_{N2} = K_{Neff} = 6.90 \times 10^{-4} (\mathrm{A/V^2})$$

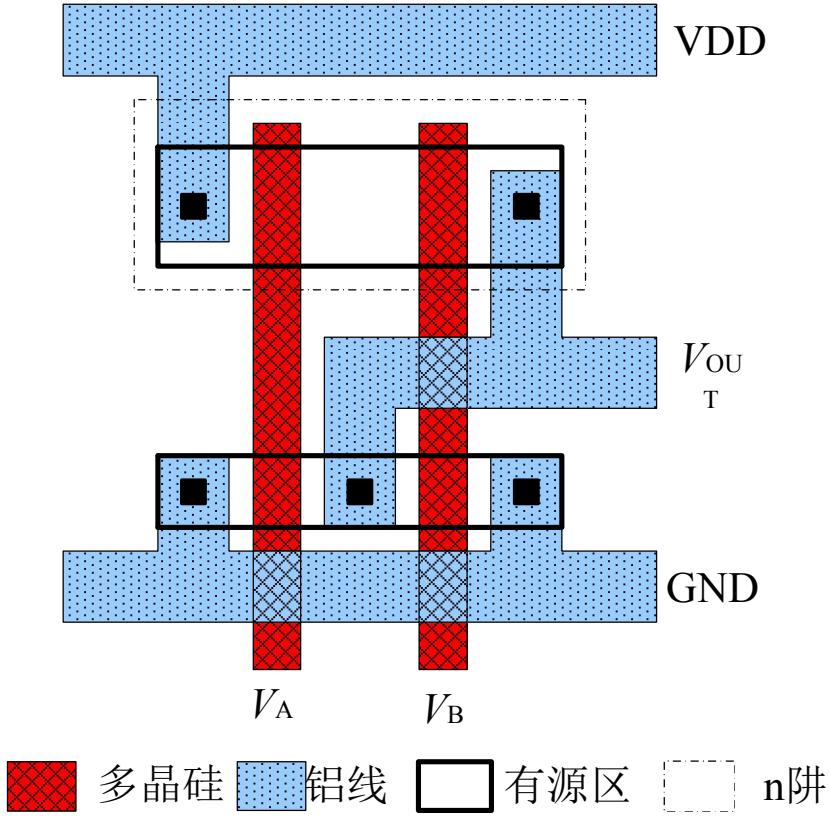
则有 $$L_N = L_P = 0.6\mu\mathrm{m}$$

$$W_{P1} = W_{P2} = 28.56 \approx 29(\mu\mathrm{m})$$

$$W_{N1} = W_{N2} = 6.9 \approx 7(\mu\mathrm{m})$$

与非门、或非门版图实例





四输入与非门