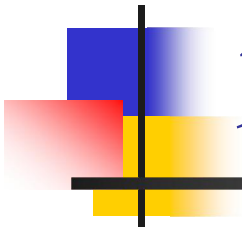
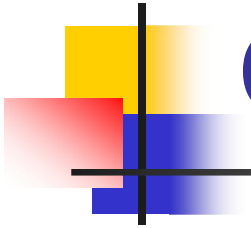


第四章 CMOS单元电路

4.3 反相器的设计

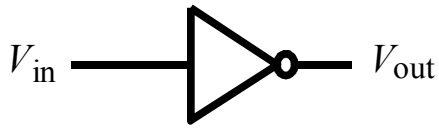


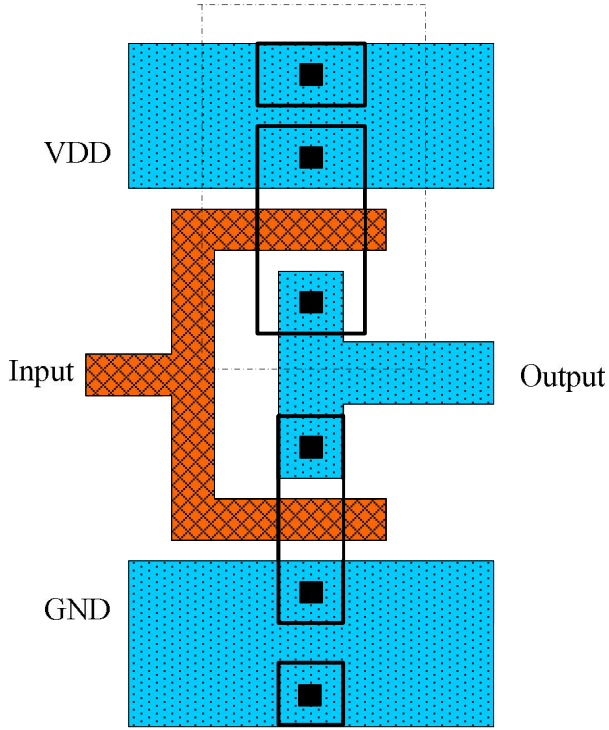
CMOS反相器

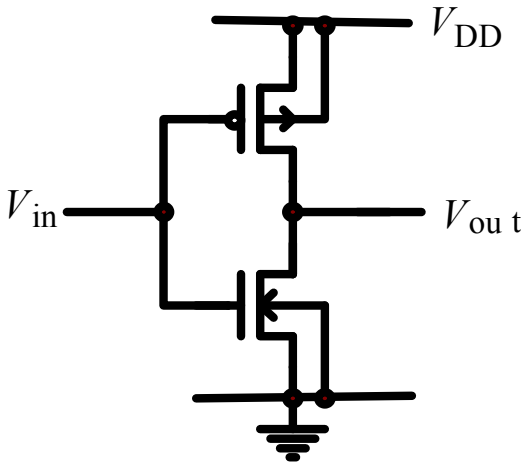
- **4.1 CMOS反相器的直流特性**
- **4.2 CMOS反相器的瞬态特性**
- **4.3 CMOS反相器的设计**

CMOS反相器

反相器的逻辑符号

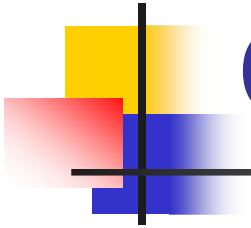






■反相器的设计变量包括**NMOS**和**PMOS**的宽度和长度

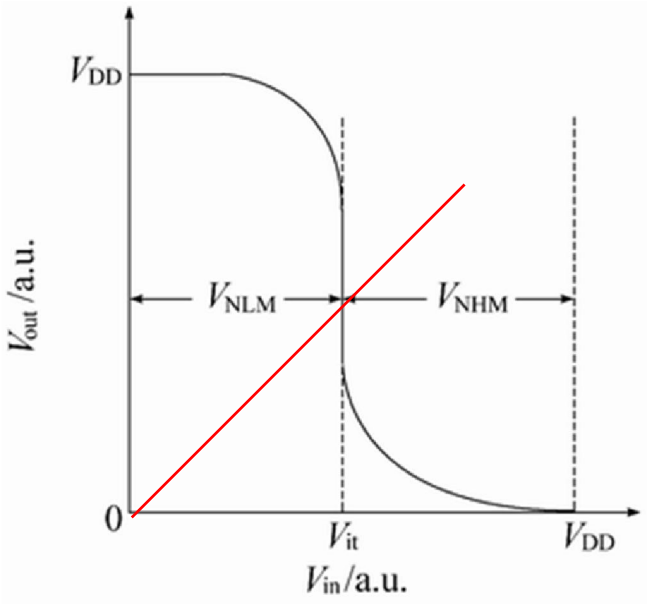
■实际的设计变量就是**NMOS**和**PMOS**的宽度（**Wp**和**Wn**）



CMOS 反相器的设计

- 完成能够实现设计要求的集成电路产品
- 设计要求：
  - 功能
  - 可靠性
  - 速度
  - 面积
  - 功耗

1、反相器的可靠性



噪声容限：逻辑阈值点

① 把V_{it}做为允许的输入高电平和低电平极限

② $V_{NLM}=V_{it}$
$V_{NHM}=V_{DD}-V_{it}$

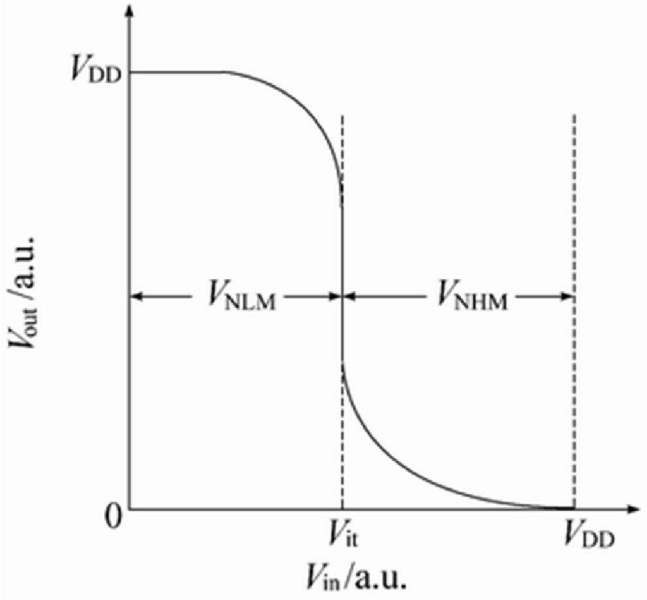
③ V_{NLM}与V_{NHM}中较小的决定最大直流噪声容限

$$V_{it}=\frac{V_{TN}+\sqrt{1/K_r}\left(V_{DD}+V_{TP}\right)}{1+\sqrt{1/K_r}}=\frac{\sqrt{K_r}V_{TN}+V_{DD}+V_{TP}}{1+\sqrt{K_r}}$$

$$V_{it}=\frac{V_{TN}+\sqrt{1/K_r}\left(V_{DD}+V_{TP}\right)}{1+\sqrt{1/K_r}}=\frac{\sqrt{K_r}V_{TN}+V_{DD}+V_{TP}}{1+\sqrt{K_r}}$$

可靠性：噪声容限

- 面向可靠性最优的设计目标，噪声容限最大就是使得**Vit=Vdd/2**



- 在反相器的设计中通过器件尺寸的设计保持电路满足噪声容限的要求

- 利用噪声容限的设计要求可以得到**Wp**和**Wn**的一个方程

2、反相器的速度

- 一般用反相器的平均延迟时间表示速度
- 也可以分别用上升和下降延迟时间表示
- 利用速度的设计要求可以得到**Wp**和**Wn**的一个方程

$$t_p = \frac{t_{pHL} + t_{pLH}}{2}$$

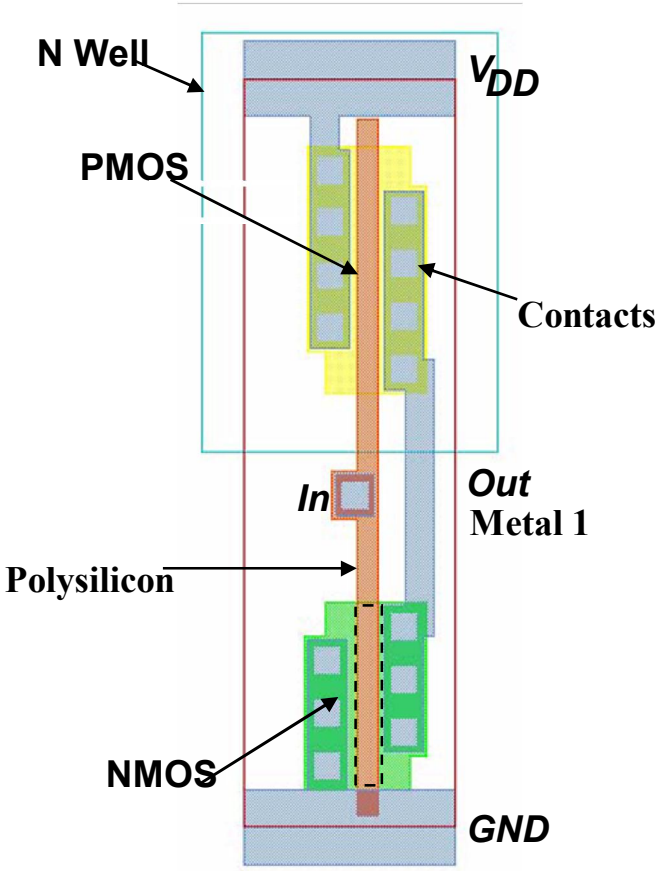
$$t_{pHL} = \frac{C_L \Delta V_{HL}}{I_{av,HL}} \approx \tau_f \frac{1}{(1-\alpha_N)^2}$$

$$t_{pLH} = \frac{C_L \Delta V_{LH}}{I_{av,LH}} \approx \tau_r \frac{1}{(1-\alpha_P)^2}$$

$$t_p = \frac{1}{2}\tau_r \left[\frac{1}{K_r (1-\alpha_N)^2} + \frac{1}{(1-\alpha_P)^2} \right]$$

3、反相器的面积

- 减小器件的宽度可以减小面积
- 例如最小面积的要求可以采用最小尺寸的器件尺寸
- 利用面积的设计要求可以得到**Wp**和**Wn**的一个方程



4、反相器的功耗

$$P_D = C_L f V_{DD}^2$$

- 增加器件宽长比会增加电容
- 电路速度增加也会提高功耗
- 电源电压的增加
- 功耗暂时不作为反相器设计的约束

$$V_{it}=\frac{V_{TN}+\sqrt{1/K_r}\left(V_{DD}+V_{TP}\right)}{1+\sqrt{1/K_r}}=\frac{\sqrt{K_r}V_{TN}+V_{DD}+V_{TP}}{1+\sqrt{K_r}}$$

反相器设计：综合

$$t_p=\frac{t_{pHL}+t_{pLH}}{2}$$

$$t_{pHL}=\frac{C_L\Delta V_{HL}}{I_{av,HL}}\approx\tau_f\frac{1}{\left(1-\alpha_N\right)^2}$$

$$t_{pLH}=\frac{C_L\Delta V_{LH}}{I_{av,LH}}\approx\tau_r\frac{1}{\left(1-\alpha_P\right)^2}$$

- 利用可靠性、速度和面积约束中的两个就可以得到一组**Wp**和**Wn**
- 对称反相器：对于**NMOS**和**PMOS**阈值基本相等的工艺，设计**Kr＝1**
- 对称反相器具有最大的噪声容限和相等的上升和下降延迟，在没有具体设计要求情况下是相对优化的设计

例　题

- 设计一个CMOS反相器，使最大噪声容限不小于0.44 V_{DD}，且驱动1pF负载电容时上升、下降时间不大于10ns，设V_{DD} = 5V，V_{TN} = 0.8V，V_{TP} = -1V，Cox = 4.6×10^{-8} F/cm^2，μn = 500 cm^2/Vs、μp = 200 cm^2/Vs。

$$V_{it}=\frac{V_{TN}+\sqrt{1/K_r}\,(V_{DD}+V_{TP})}{1+\sqrt{1/K_r}}=\frac{\sqrt{K_r}V_{TN}+V_{DD}+V_{TP}}{1+\sqrt{K_r}}$$

$$t_r=\tau_r\left[\frac{\alpha_P-0.1}{(1-\alpha_P)^2}+\frac{1}{2(1-\alpha_P)}\ln\left(\frac{1.9-2\alpha_P}{0.1}\right)\right]$$

$$\tau_r=\frac{C_L}{K_P V_{DD}}$$

$\alpha_N=V_{TN}/V_{DD}=0.16$, $\alpha_P=-V_{TP}/V_{DD}=0.2$

则 $t_r=1.85\tau_r=10ns$, $\tau_r=5.4ns$

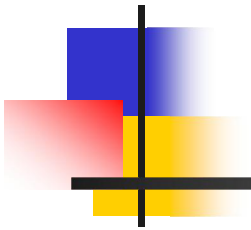
得到：$K_P=3.7\times10^{-5}\,(A/V^2)$ $\left(\frac{W}{L}\right)_P\approx 8$

同理得到：$t_f=1.73\tau_f=10ns$, $\tau_f=5.78ns$

$K_N=3.46\times10^{-5}\,(A/V^2)$, $\left(\frac{W}{L}\right)_N\approx 3$

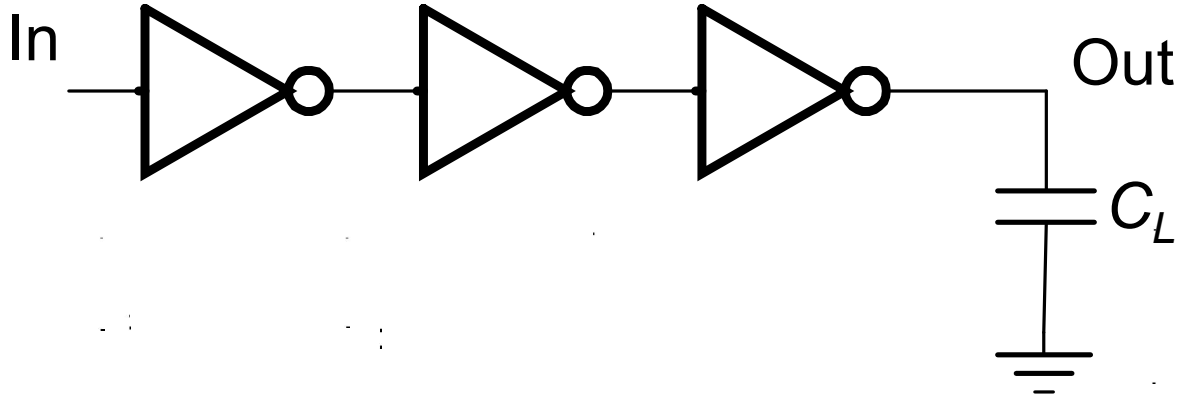
考察噪声容限：$V_{NLM}=V_{it}=2.43V=0.49\,V_{DD}$,

$V_{NHM}=V_{DD}-V_{it}=2.57V=0.51\,V_{DD}$



反相器链的设计

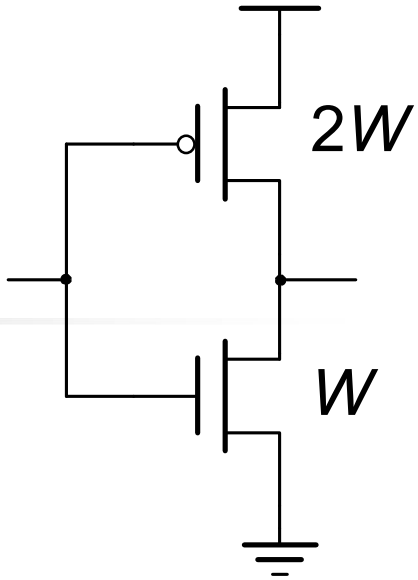
反相器链



当电路扇出（负载电容）较大的时候，如何有效进行驱动

如果负载电容给定：
则为了获得最小**In**到**Out**的延迟，应该用多少级反相器，
如何确定每级反相器的器件尺寸？

Inverter Delay



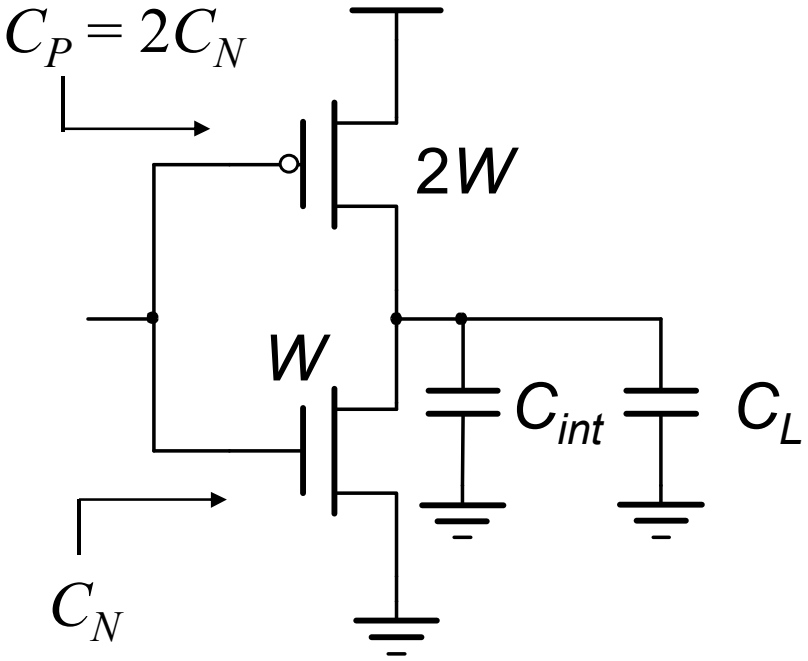
- 采用对称反相器
- **$W_P = 2W_N = 2W$**
  - **approx. equal resistances $R_N = R_P$**
  - **approx. equal rise t_{pLH} and fall t_{pHL} delays**

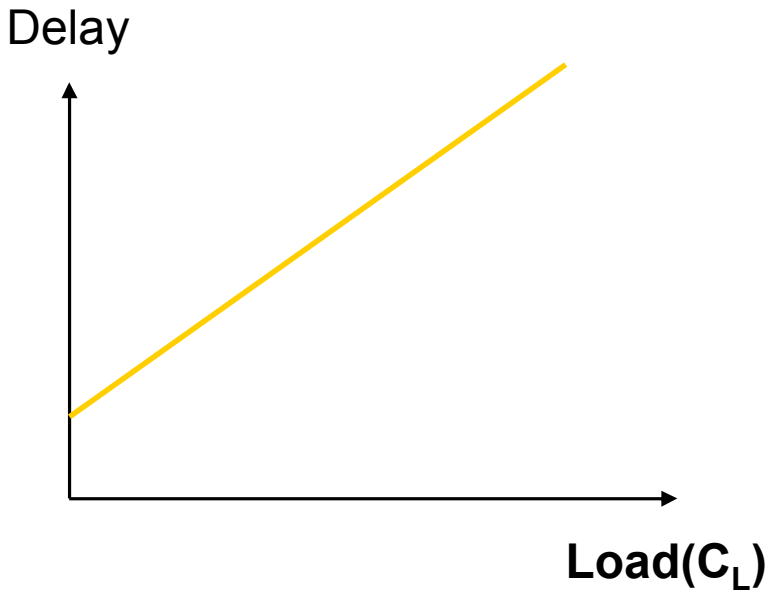
$$R_P = R_N = R_W$$

Delay (*D*): $t_{pHL} = (\ln 2)\, R_N C_L$ $\qquad$ $t_{pLH} = (\ln 2)\, R_P C_L$

栅电容: $\qquad C_{gin} = 3\dfrac{W}{W_{unit}} C_{unit}$

Inverter with Load



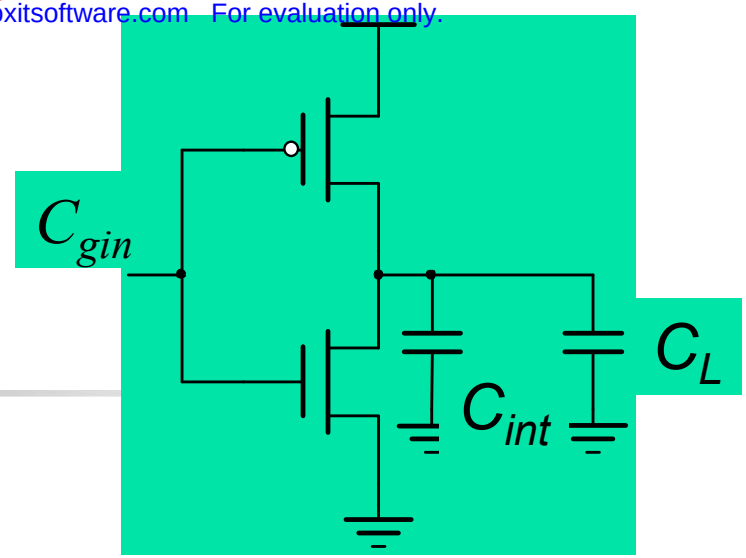


Delay = $0.69R_W(C_{int} + C_L) = 0.69R_W C_{int}(1 + C_L / C_{int})$

Delay (Internal) + Delay (Load)

Delay Formula

$$Delay \sim R_W \left(C_{int} + C_L \right)$$



$$t_p = 0.69 R_W C_{\text{int}} \left(1 + C_L / C_{int}\right) = t_{p0}\left(1 + f / \gamma\right)$$

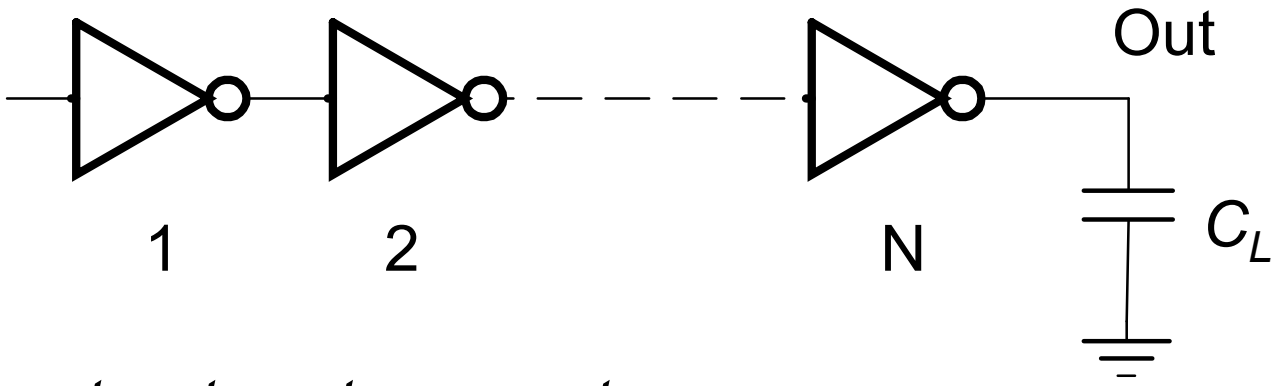
$C_{int} = \gamma C_{gin}$ with $\gamma \approx 1$

$f = C_L / C_{gin}$ - effective fanout

反相器的本征延迟：**$t_{p0} = 0.69 R_w C_{int}$**

$$R_P = R_N = R_W \qquad C_{gin} = 3\frac{W}{W_{unit}} C_{unit}$$

Apply to Inverter Chain

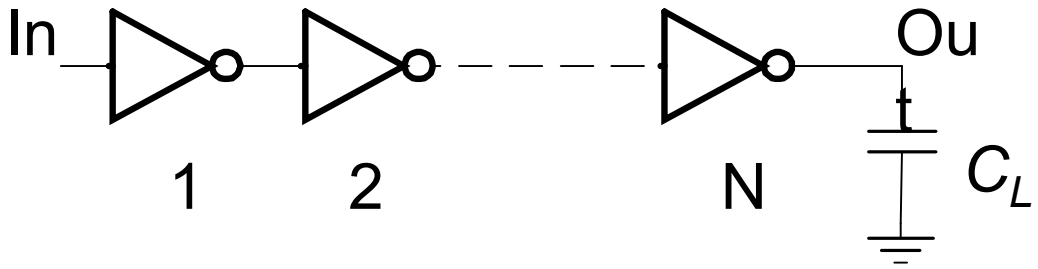


$$t_p = t_{p1} + t_{p2} + \ldots + t_{pN}$$

$$t_{pj} \sim R_W C_{\text{int}} \left(1 + \frac{C_{gin,j+1}}{\gamma C_{gin,j}} \right)$$

$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{i=1}^{N} \left(1 + \frac{C_{gin,j+1}}{\gamma C_{gin,j}} \right), \quad C_{gin,N+1} = C_L$$

Optimal Tapering for Given *N*



Delay equation has $N - 1$ unknowns, $C_{gin,2} - C_{gin,N}$

Minimize the delay, find $N - 1$ partial derivatives

Result: $C_{gin,j+1}/C_{gin,j} = C_{gin,j}/C_{gin,j-1}$

Size of each stage is the geometric mean of two neighbors

$$C_{gin,j} = \sqrt{C_{gin,j-1}C_{gin,j+1}}$$

- each stage has the same effective fanout ($f = C_{out}/C_{in}$)
- each stage has the same delay

$$t_p = t_{p0}\left(1 + f/\gamma\right)$$

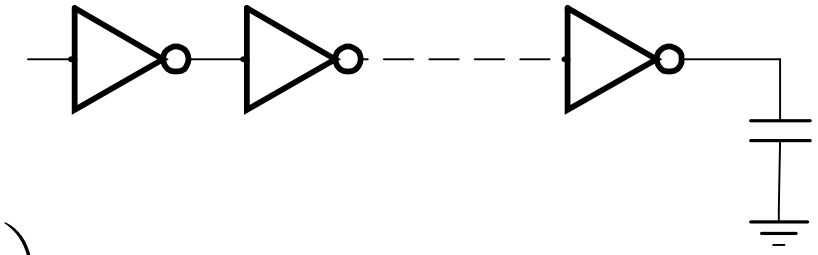
Optimum Delay and Number of Stages

When each stage is sized by *f* and has same eff. fanout *f*:

$$f^N = F = C_L / C_{gin,1}$$

最优扇出**f**：

$$f = \sqrt[N]{F}$$



$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{i=1}^{N} \left(1 + \frac{C_{gin,j+1}}{\gamma C_{gin,j}} \right), \quad C_{gin,N+1} = C_L$$

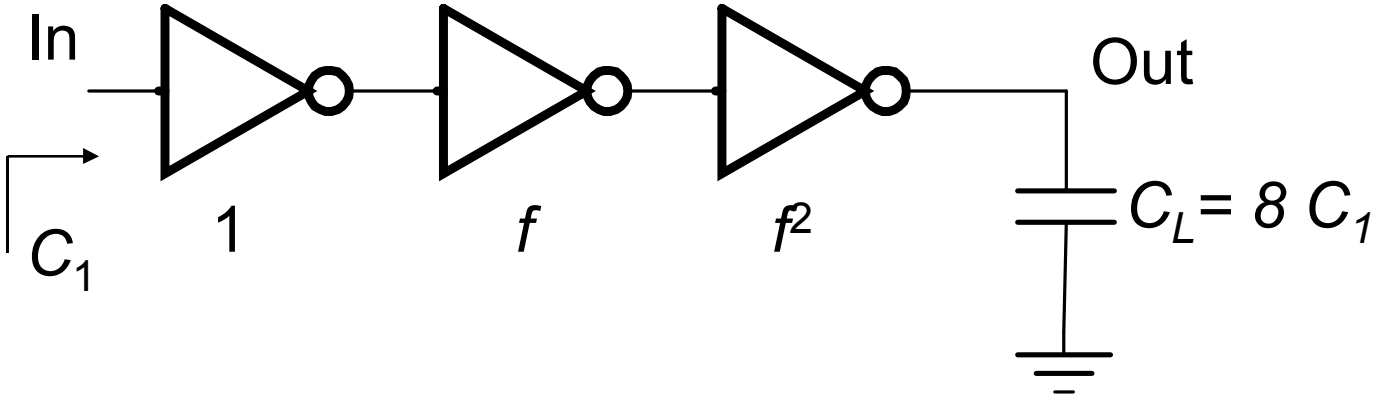
反相器链最优延迟

$$t_p = N t_{p0} \left(1 + \sqrt[N]{F} / \gamma \right)$$

$$f = \sqrt[N]{F}$$

Example

$$t_p = Nt_{p0}\left(1 + \sqrt[N]{F}/\gamma\right)$$



如果采用3级反相器驱动负载电容，则每级反相器的尺寸应该逐次增加f倍

$$f = \sqrt[3]{8} = 2$$

扇出f的最优值

$$t_p = Nt_{p0}\left(1+\sqrt[N]{F}/\gamma\right)$$

对于给定负载电容 C_L 和确定的第一级反相器的输入电容C_{in}*可以找到f的最优值，并由此确定反相器级数N的最优值*

$$C_L = F\cdot C_{in} = f^N C_{in} \quad \text{with} \quad N = \frac{\ln F}{\ln f}$$

$$t_p = Nt_{p0}\left(F^{1/N}/\gamma+1\right) = \frac{t_{p0}\ln F}{\gamma}\left(\frac{f}{\ln f}+\frac{\gamma}{\ln f}\right)$$

$$\frac{\partial t_p}{\partial f} = \frac{t_{p0}\ln F}{\gamma}\cdot\frac{\ln f - 1 - \gamma/f}{\ln^2 f} = 0$$

$C_{int} = \gamma C_{gin}$

$$f = \exp\left(1+\gamma/f\right)$$

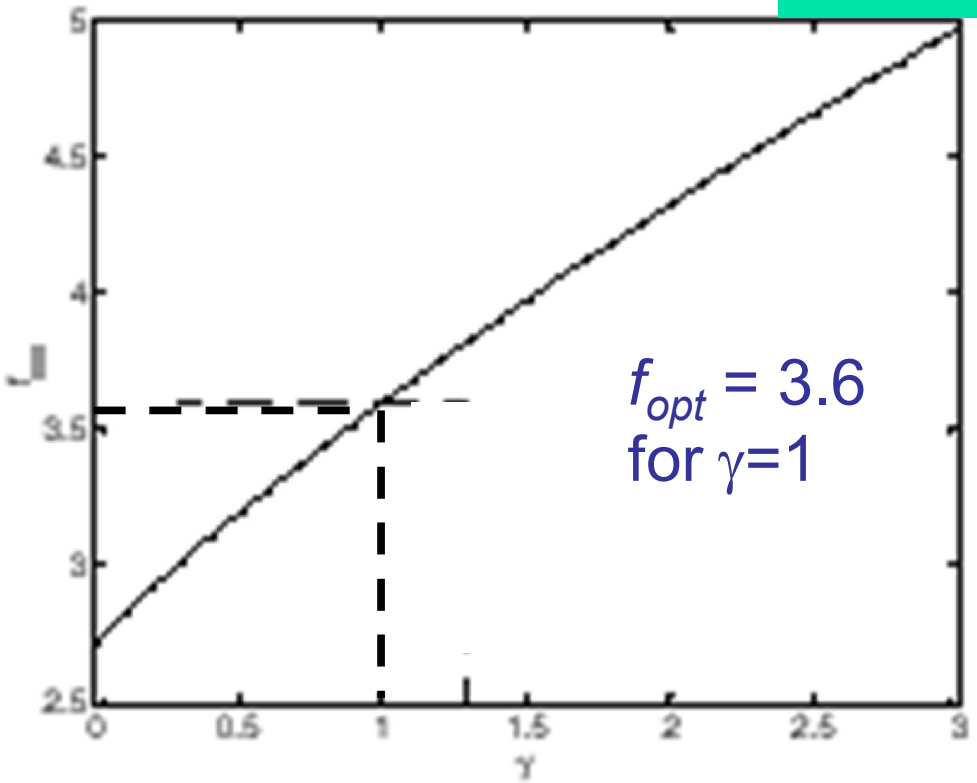
对于 $\gamma = 0$, 即忽略Cint，
则有$f = e$, $N = \ln F$

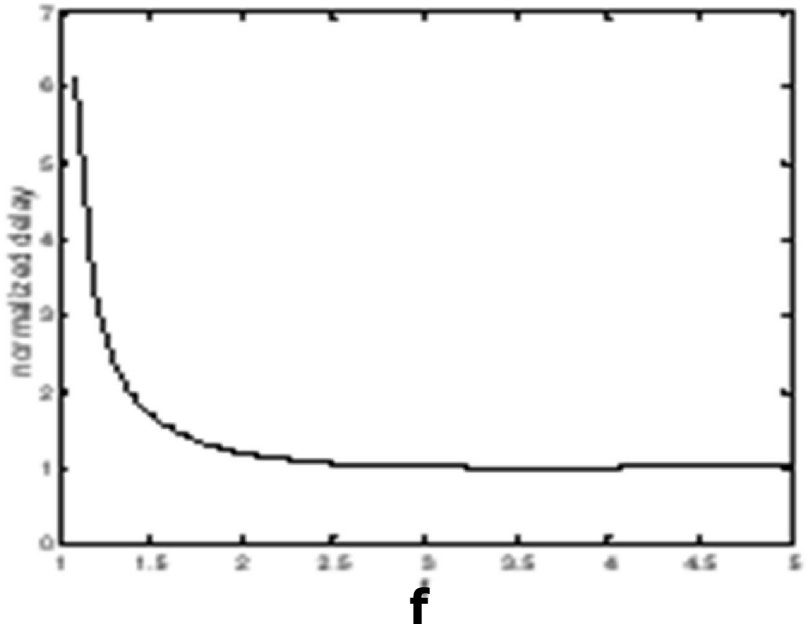
Optimum Effective Fanout *f*

对于考虑漏区负载电容情况，即 γ不等于0的时候

$$f = \exp(1+\gamma/f)$$

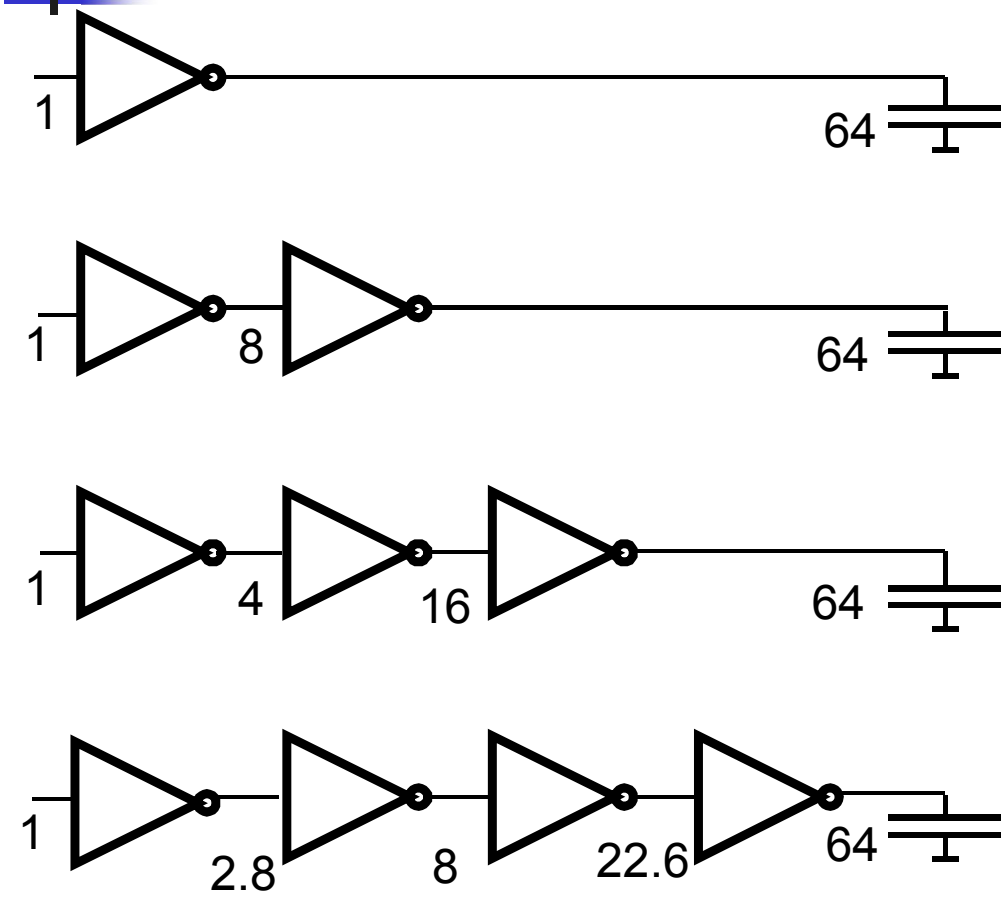
$$t_p = Nt_{p0}\left(F^{1/N}/\gamma+1\right)=\frac{t_{p0}\ln F}{\gamma}\left(\frac{f}{\ln f}+\frac{\gamma}{\ln f}\right)$$





$$t_p = Nt_{p0}\left(1 + \sqrt[N]{F}/\gamma\right)$$

Buffer Design



N	f	t_p
1	64	65
2	8	18
3	4	15
4	2.8	15.3

Normalized delay function of *F*

$$t_p = Nt_{p0}\left(1 + \sqrt[N]{F}/\gamma\right)$$

F	Unbuffered	Two Stage	Inverter Chain
10	11	8.3	8.3
100	101	22	16.5
1000	1001	65	24.8
10,000	10,001	202	33.1