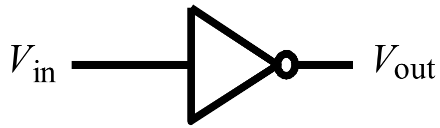
第四章 CMOS单元电路

4.1 反相器直流特性

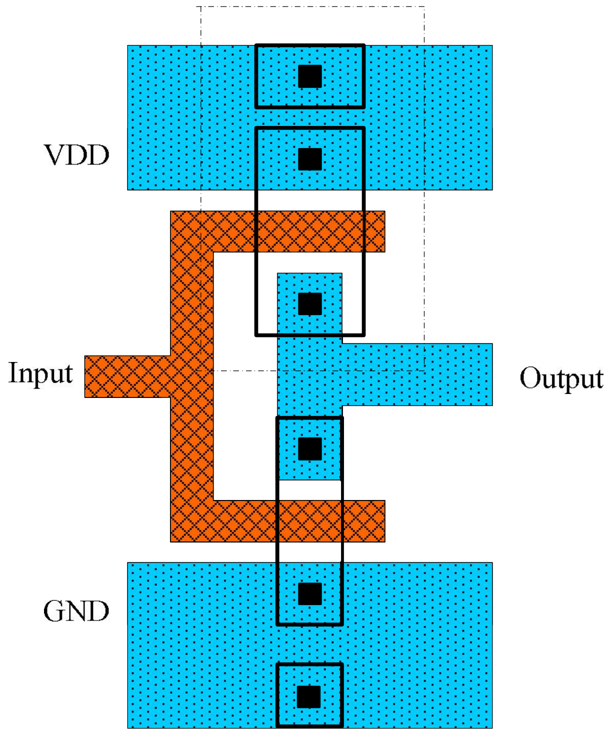
CMOS反相器

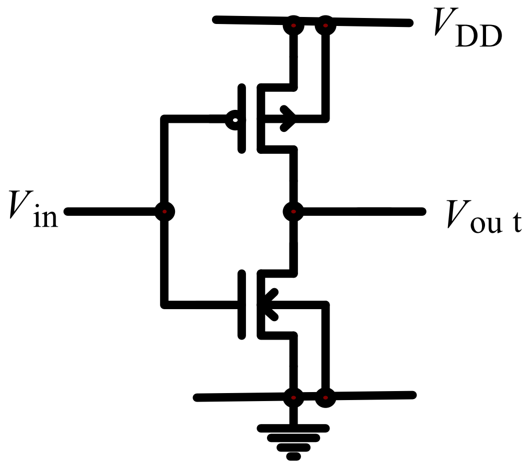
- 4.1 CMOS反相器的直流特性
- 4.2 CMOS反相器的瞬态特性
- 4.3 CMOS反相器的设计

反相器的逻辑符号



CMOS Inverter





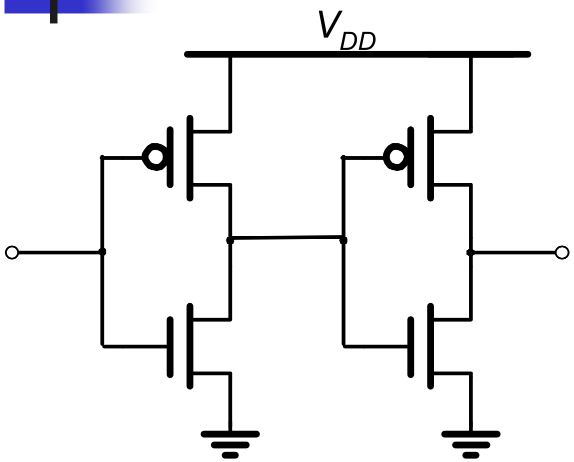
特点:

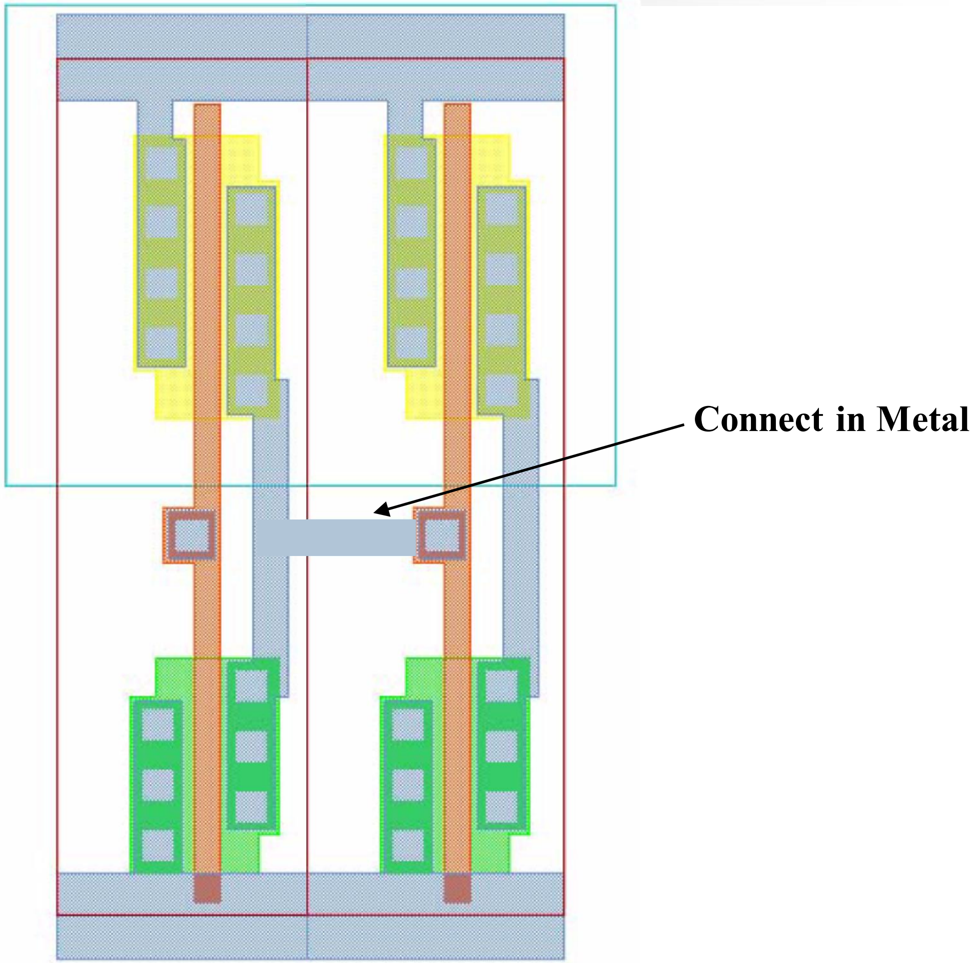
Vin作为PMOS和NMOS的共栅极;
Vout作为共漏极;
VDD作为PMOS的源极和体端;
GND作为NMOS的源极和体端

Two Inverters

Share power and ground

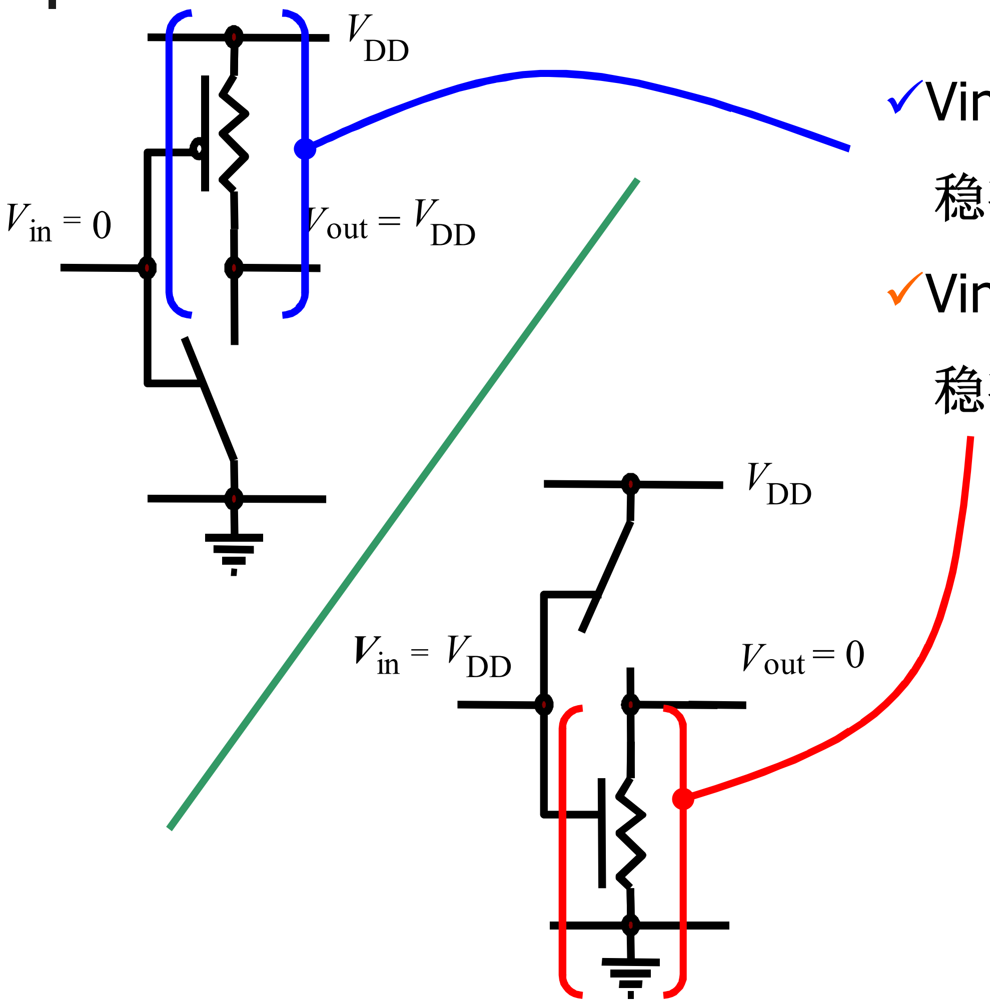
Abut cells





- ➢标准单元形式的门电路的版图设计
- ➢通过等高的设计共享电源和地线
- ➢通过邻接的设计减小面积

CMOS反相器的直流特性



✓Vin=0，NMOS截止，PMOS导通，

稳态Vout= VDD ,“1”；

✓Vin= VDD，NMOS导通，PMOS截止，

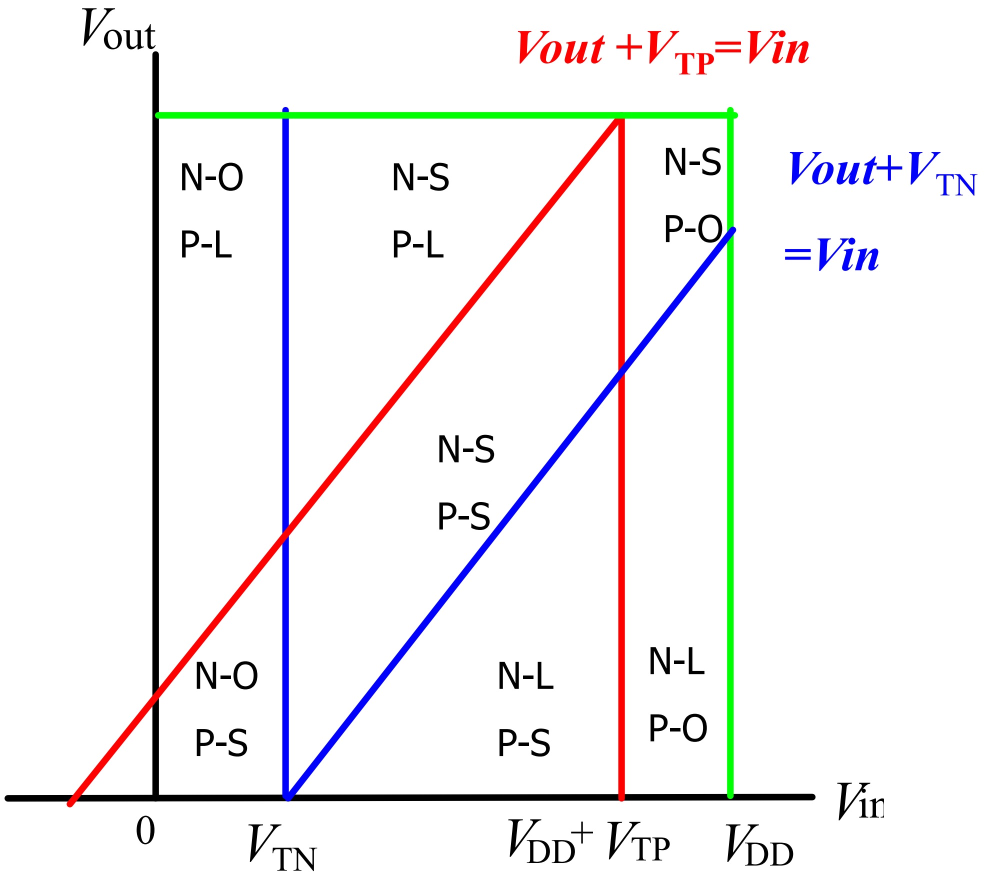
稳态Vout=0；

反相器的工作特点：

✓ ***$Vout=\overline{Vin}$;***

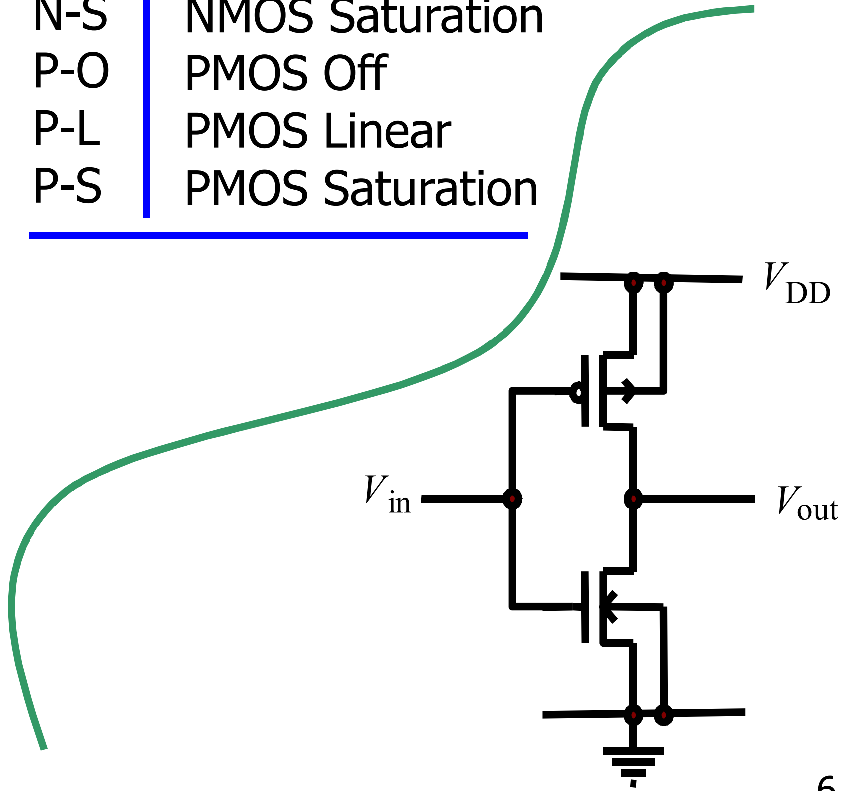
✓稳态单管导通，没有直通电流

反相器中*MOSFET*的工作区域

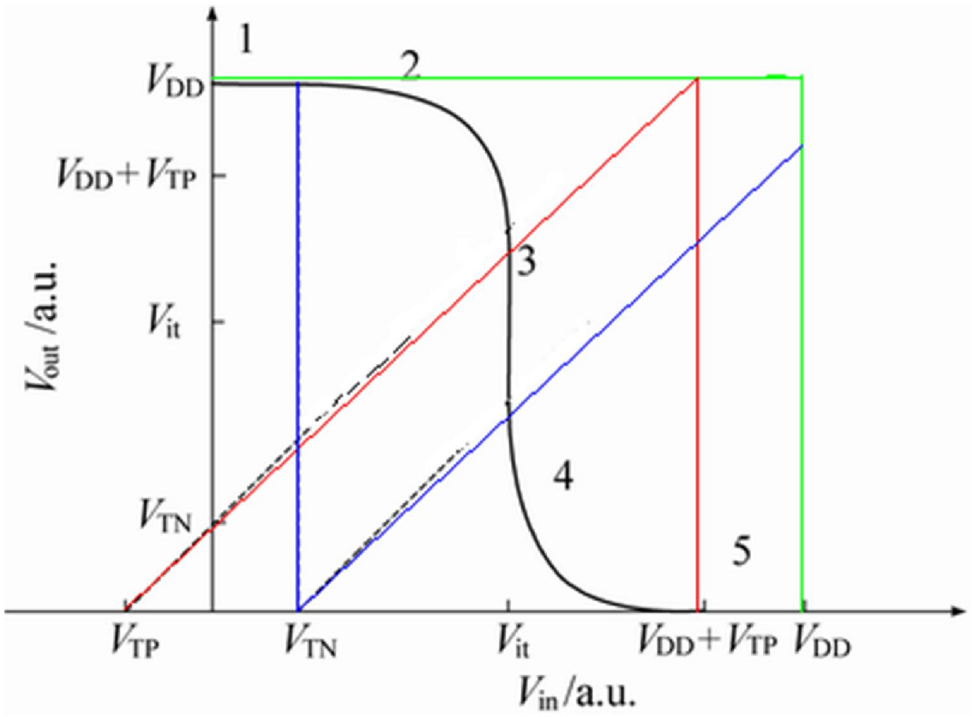


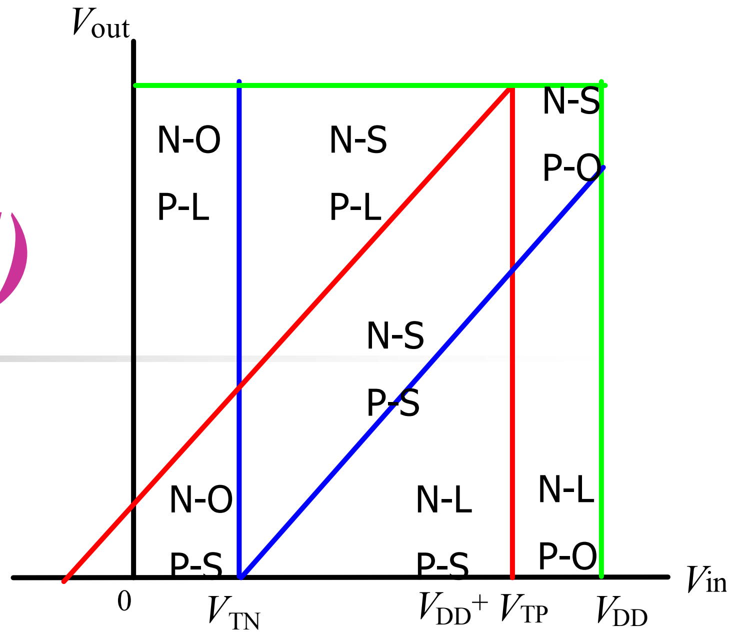
缩写对照：

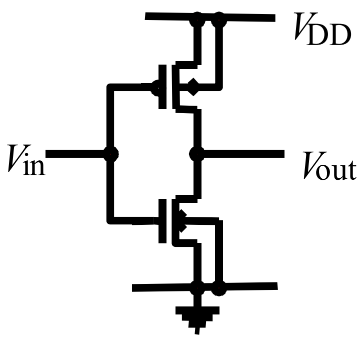
N-O	NMOS Off
N-L	NMOS Linear
N-S	NMOS Saturation
P-O	PMOS Off
P-L	PMOS Linear
P-S	PMOS Saturation



Voltage Transfer Characteristic(VTC)

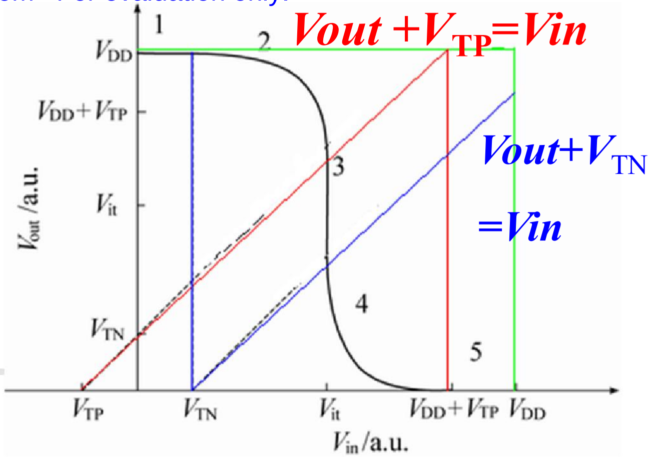






分析直流特性的出发点：
直流条件下没有输出电流
满足：$I_{DN}=I_{DP}$

1、反相器的VTC



1、 $0 \le V_{\text{in}} \le V_{\text{TN}}$ 特点：***N-O & P-L***

$$I_{DP} = K_P\left[\left(V_{in} - V_{TP} - V_{DD}\right)^2 - \left(V_{in} - V_{TP} - V_{out}\right)^2\right] = I_{DN} = 0$$

$$V_{out} = V_{DD}, \qquad \therefore \quad V_{OH} = V_{DD}$$

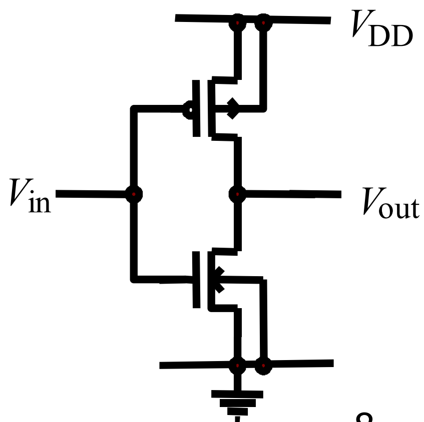
2、 $V_{\text{TN}} < V_{\text{in}} < V_{\text{out}} + V_{\text{TP}}$ 特点： ***N-S & P-L***

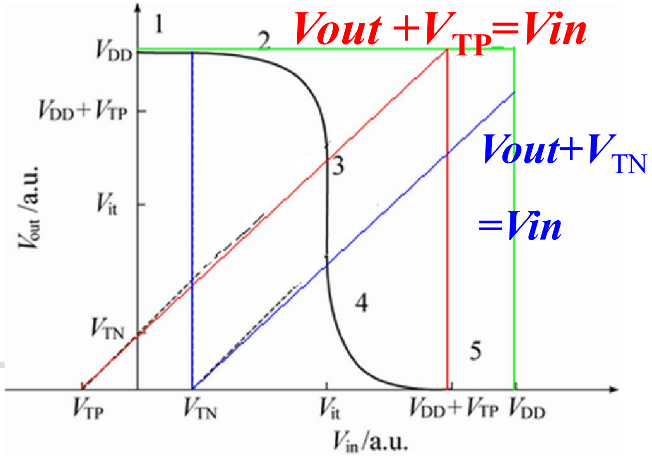
$$K_P\left[\left(V_{in} - V_{TP} - V_{DD}\right)^2 - \left(V_{in} - V_{TP} - V_{out}\right)^2\right] = K_N\left(V_{in} - V_{TN}\right)^2$$

$$V_{out} = \left(V_{in} - V_{TP}\right) + \left[\left(V_{in} - V_{TP} - V_{DD}\right)^2 - K_r\left(V_{in} - V_{TN}\right)^2\right]^{1/2}$$

$$K_r = K_N / K_P$$

比例因子





反相器VTC

3、 $V_{out}+V_{TP}\le V_{in}\le V_{out}+V_{TN}$ 特点：***N-S & P-S***

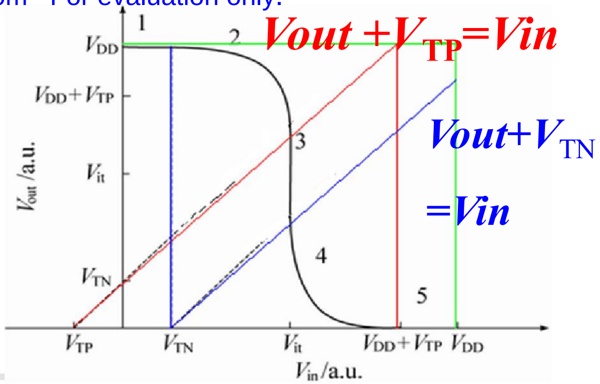
$$K_N\left(V_{in}-V_{TN}\right)^2=K_P\left(V_{in}-V_{TP}-V_{DD}\right)^2$$

$$V_{in}=\frac{V_{TN}+\sqrt{1/K_r}\left(V_{DD}+V_{TP}\right)}{1+\sqrt{1/K_r}}$$

$$V_{it}=\frac{V_{TN}+\sqrt{1/K_r}\left(V_{DD}+V_{TP}\right)}{1+\sqrt{1/K_r}}=\frac{\sqrt{K_r}V_{TN}+V_{DD}+V_{TP}}{1+\sqrt{K_r}}$$

反相器的逻辑阈值电平（逻辑转折点）

反相器VTC



4、 $V_{out} + V_{TN} < V_{in} < V_{DD} + V_{TP}$ 特点：***N-L & P-S***

$$K_N\left[(V_{in}-V_{TN})^2-(V_{in}-V_{TN}-V_{out})^2\right]=K_P(V_{in}-V_{TP}-V_{DD})^2$$

$$V_{out}=(V_{in}-V_{TN})-\left[(V_{in}-V_{TN})^2-\frac{1}{K_r}(V_{in}-V_{TP}-V_{DD})^2\right]^{1/2}$$

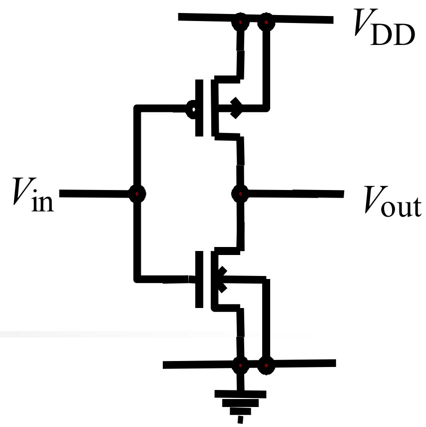
5、 $V_{DD} \ge V_{in} \ge V_{DD} + V_{TP}$ 特点： ***N-L & P-O***

$$K_N\left[(V_{in}-V_{TN})^2-(V_{in}-V_{TN}-V_{out})^2\right]=I_{DP}=0$$

$$V_{out}=0 \quad \therefore \quad V_{OL}=0$$

CMOS反相器实现全摆幅

器件参数对VTC的影响



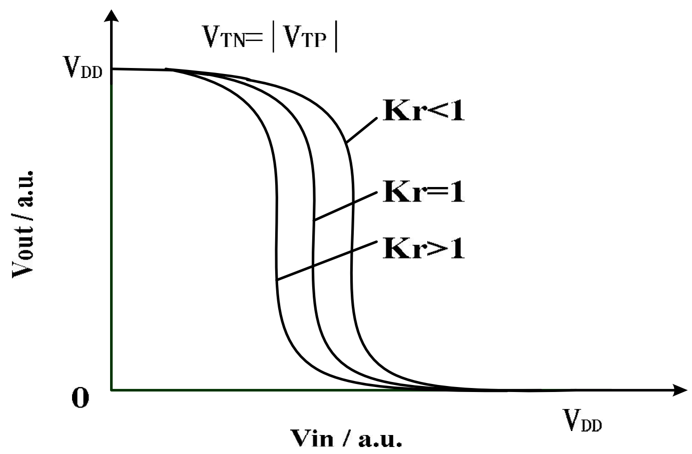
$$V_{in} = \frac{V_{TN} + \sqrt{1/K_r}\,(V_{DD} + V_{TP})}{1 + \sqrt{1/K_r}}$$

$$V_{it} = \frac{V_{TN} + \sqrt{1/K_r}\,(V_{DD} + V_{TP})}{1 + \sqrt{1/K_r}} = \frac{\sqrt{K_r}\,V_{TN} + V_{DD} + V_{TP}}{1 + \sqrt{K_r}}$$

反相器比例因子对直流特性的影响：

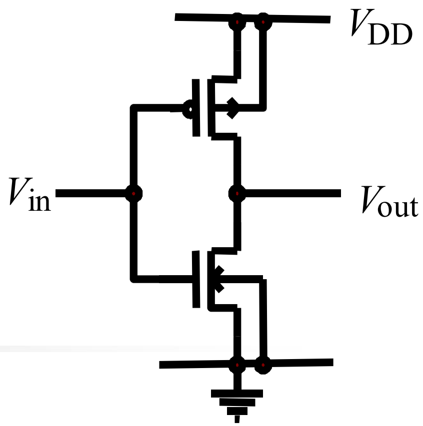
在$V_{TN}=-V_{TP}$前提下进行考虑，

以便简化问题；



(a) 导电因子的影响

器件参数对VTC的影响

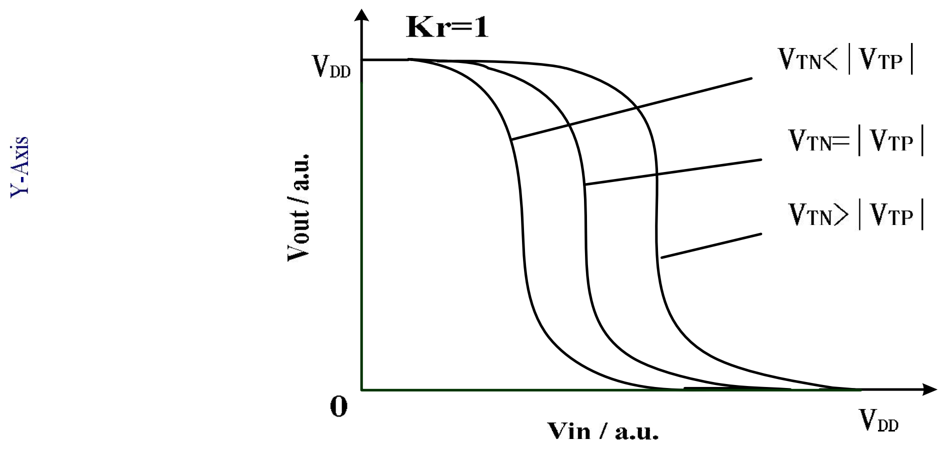


$$V_{in}=\frac{V_{TN}+\sqrt{1/K_r}\left(V_{DD}+V_{TP}\right)}{1+\sqrt{1/K_r}}$$

$$V_{it}=\frac{V_{TN}+\sqrt{1/K_r}\left(V_{DD}+V_{TP}\right)}{1+\sqrt{1/K_r}}=\frac{\sqrt{K_r}V_{TN}+V_{DD}+V_{TP}}{1+\sqrt{K_r}}$$

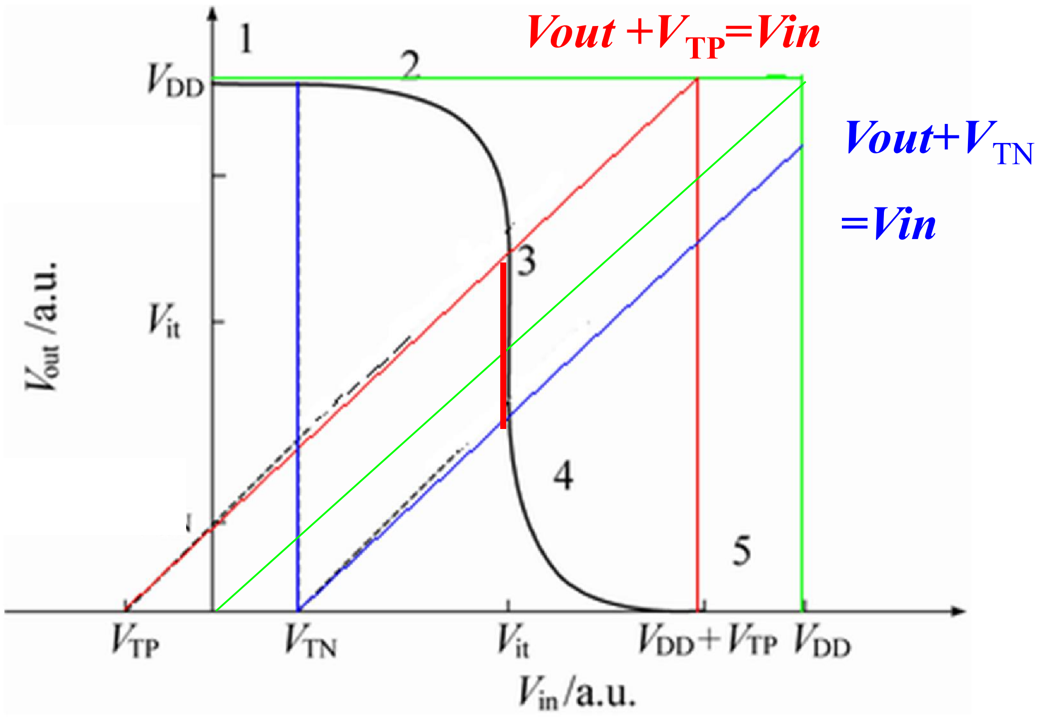
NMOS、PMOS阈值电压的影响；

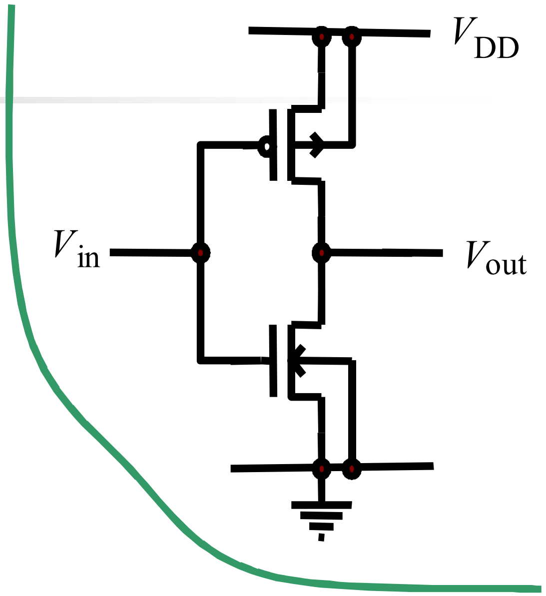
在Kr=1前提下进行考虑，以便简化问题



(b) 阈值电压的影响

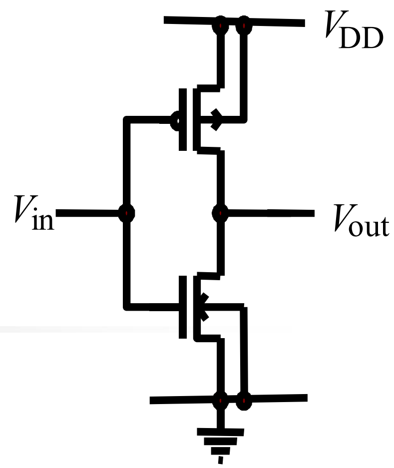
Voltage Transfer Characteristic(VTC)

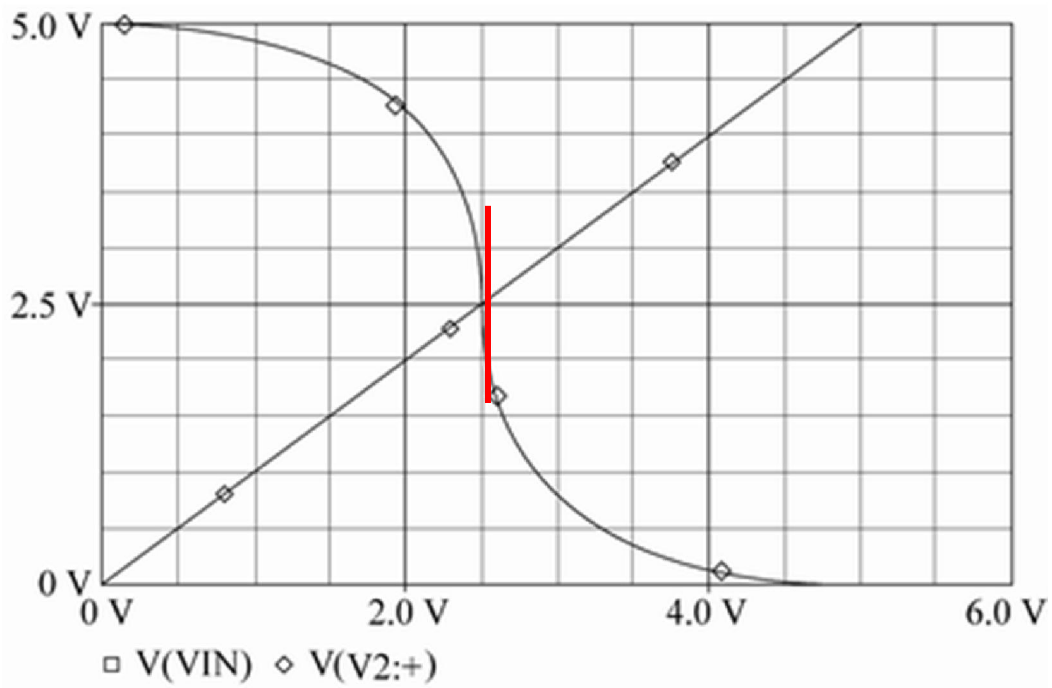




3区的高度为两个阈值之和

实际CMOS反相器的VTC





对应**Vit**的输入，输出不是一条垂直线

直流转移特性

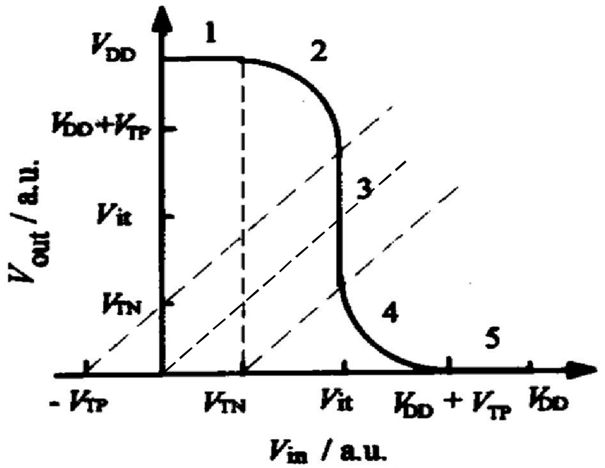
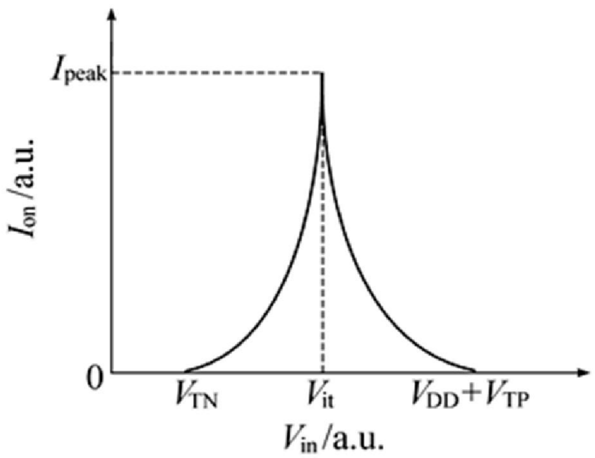


图 4.1.4 理想 CMOS 反相器的直流电压传输特性曲线



分段讨论Inverter的导通电流

1. $Vin <= V_{TN}$

   $I_{on}=I_{DN}=I_{DP}=0$,

2. $V_{TN} < Vin < Vout-|V_{TP}|$

   $I_{on}=I_{DN}=I_{DP}$ UP

3. $Vin=Vit$

   $I_{on}=I_{peak}$ at Vin=Vit

4. $Vout+V_{TN} < Vin < V_{DD}-|V_{TP}|$

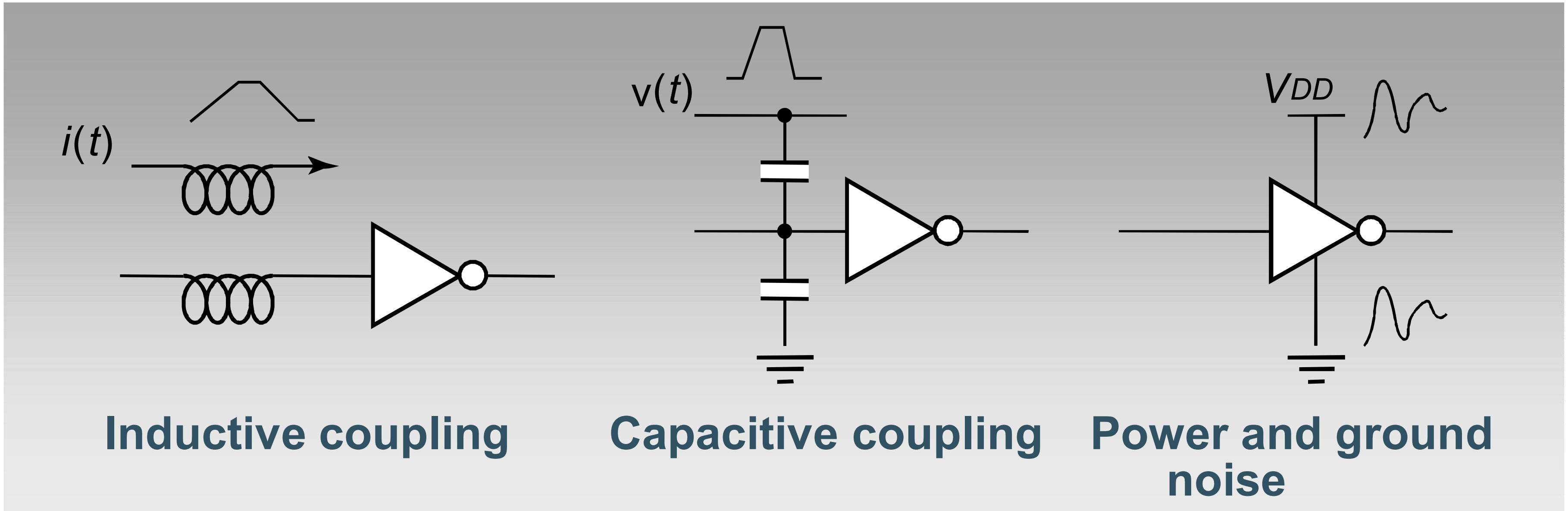
   $I_{on}=I_{DN}=I_{DP}$ DOWN

5. $V_{DD}-|V_{TP}| < Vin < V_{DD}$

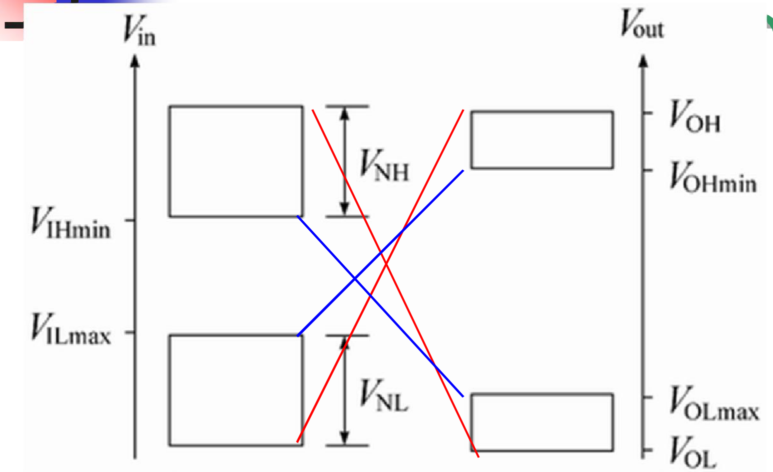
   $I_{on}=I_{DN}=I_{DP}=0$,

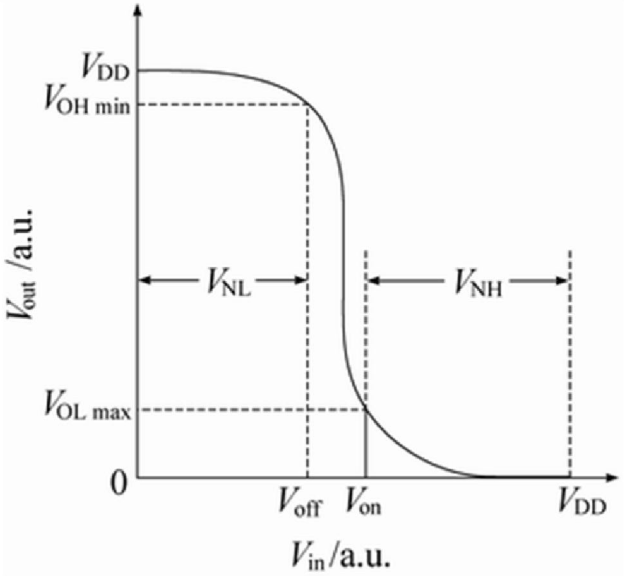
2、反相器的直流噪声容限

- 数字电路中信号在Vdd和Gnd之间转换，各种干扰信号，可能使得电路中某些结点的信号电平偏离理想电平（Vdd，Gnd），产生所谓的噪声
- 噪声会对电路的可靠性造成影响



反相器噪声容限(Noise Margins)





电路的直流噪声容限——

允许的输入电平变化范围，
反映了电路的抗干扰能力

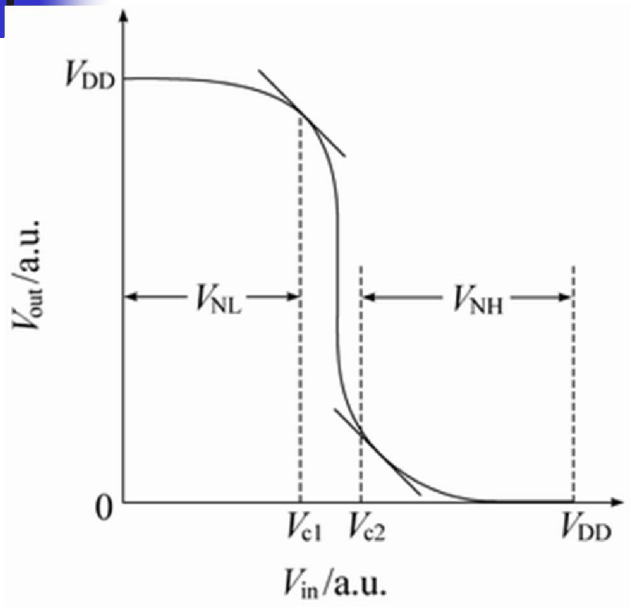
噪声容限定义1： 极限输出

① 给定V_{OHmin}和V_{OLmax}

② V_{OHmin} ➡ Voff (关门电平)
V_{OLmax} ➡ Von (开门电平)

$V_{NL}= V_{off}$, $V_{NH}=V_{DD}- V_{on}$

反相器的直流噪声容限



噪声容限定义2：单位增益点

① 在2、4区存在 |dVout/dVin|=1的单位增益点

② 在2、4区求得增益点对应的Vin (分别为Vc1和Vc2)，

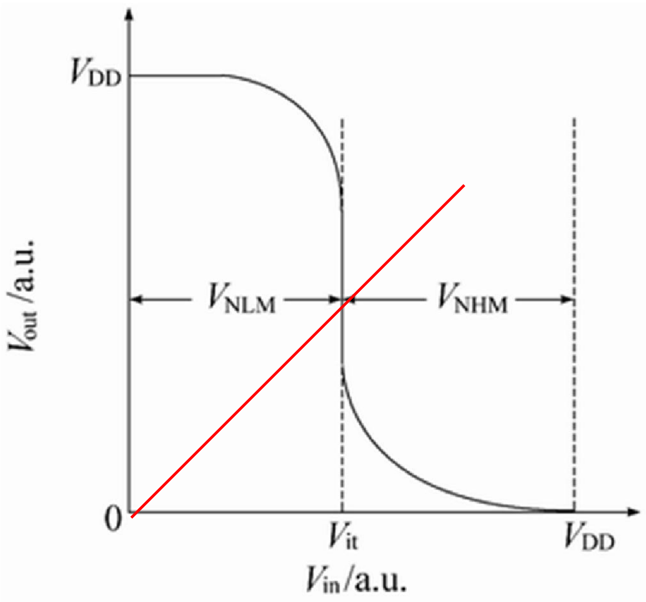
③ VNL=Vc1
VNH=VDD-Vc2

$$V_{c1}=\frac{3}{8}V_{DD}+\frac{1}{4}V_T$$

$$V_{c2}=\frac{5}{8}V_{DD}-\frac{1}{4}V_T$$

$$V_{out}=(V_{in}-V_{TP})+\left[(V_{in}-V_{TP}-V_{DD})^2-K_r(V_{in}-V_{TN})^2\right]^{1/2}$$

反相器的直流噪声容限



噪声容限定义3：逻辑阈值点

① **把Vit做为允许的输入高电平和低电平极限**

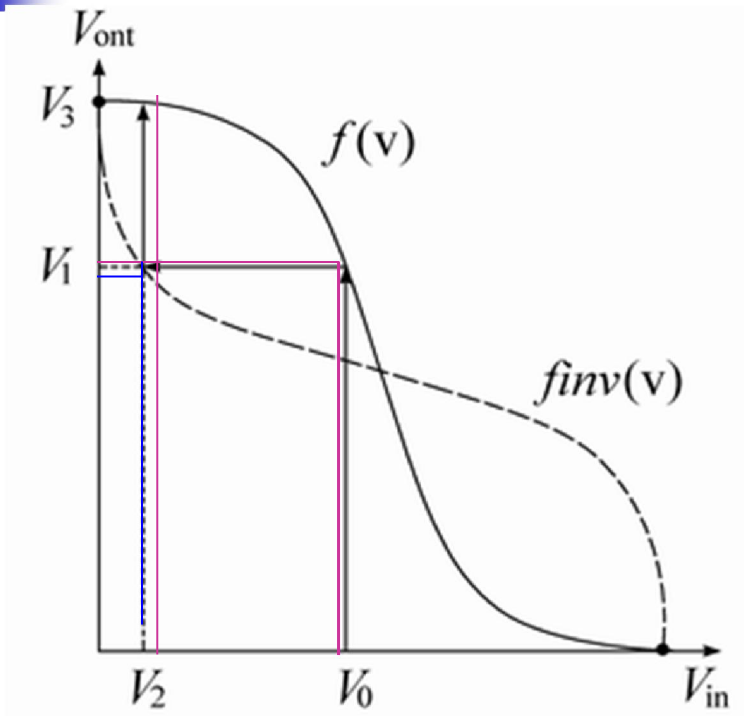
② **VNLM=Vit**
VNHM=VDD-Vit

③ **VNLM与VNHM中较小的决定最大直流噪声容限**

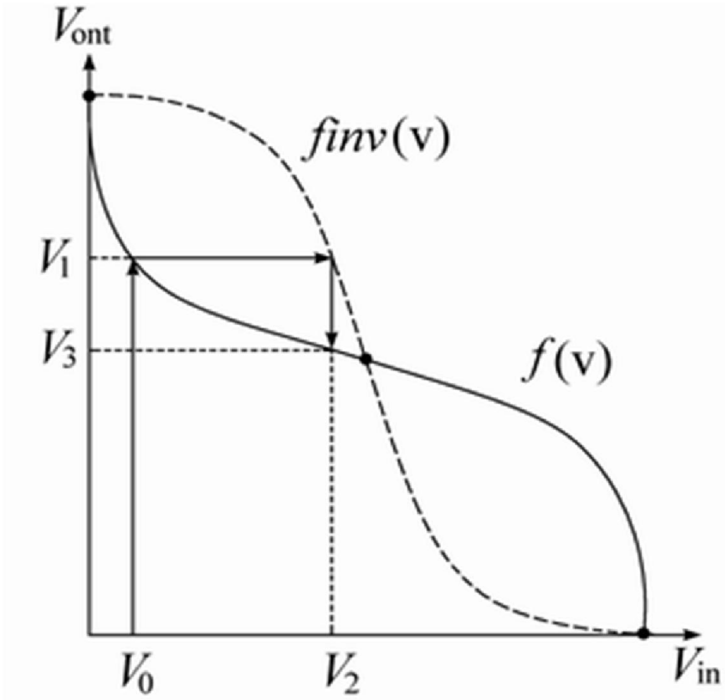
$$V_{in}=\frac{V_{TN}+\sqrt{1/K_r}\left(V_{DD}+V_{TP}\right)}{1+\sqrt{1/K_r}}$$

$$V_{it}=\frac{V_{TN}+\sqrt{1/K_r}\left(V_{DD}+V_{TP}\right)}{1+\sqrt{1/K_r}}=\frac{\sqrt{K_r}V_{TN}+V_{DD}+V_{TP}}{1+\sqrt{K_r}}$$

数字电路具有可恢复逻辑特性



可恢复逻辑特性



不可恢复逻辑特性