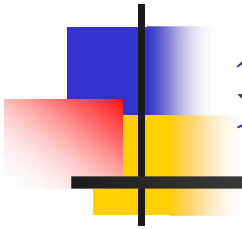


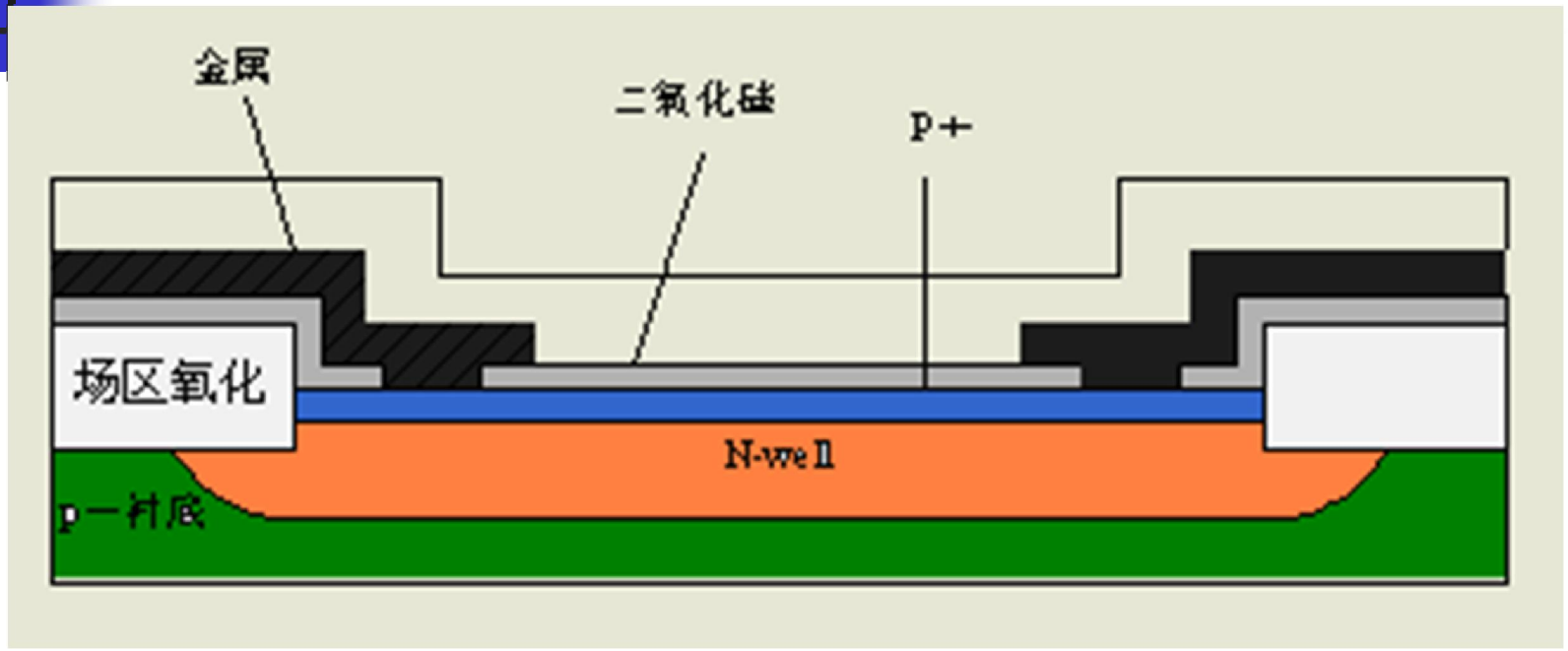
集成电路原理与设计

3.3 无源器件

CMOS工艺:无源器件

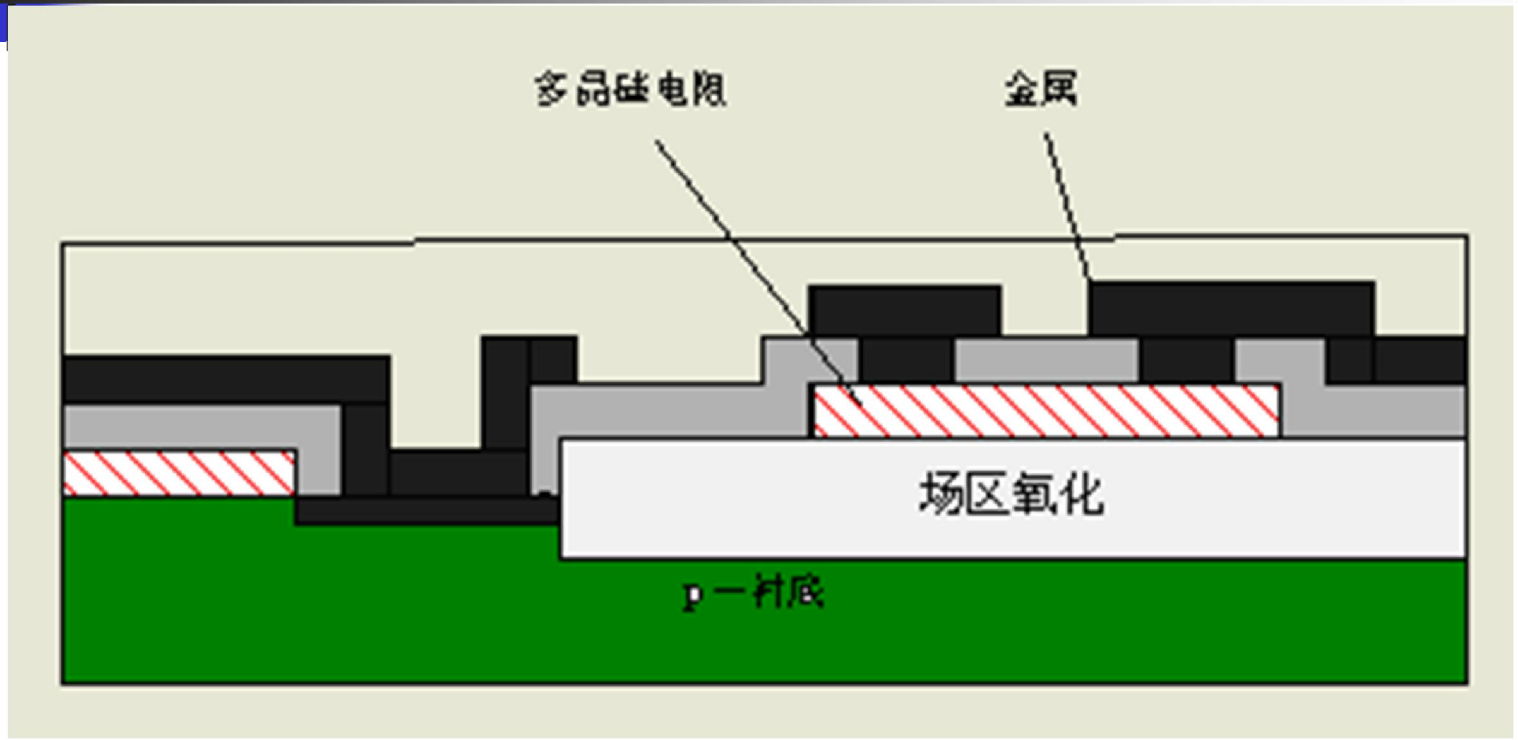
- 集成电阻器
- 集成电容器
- 集成电路中的互连线

MOS工艺： n+或p+扩散电阻



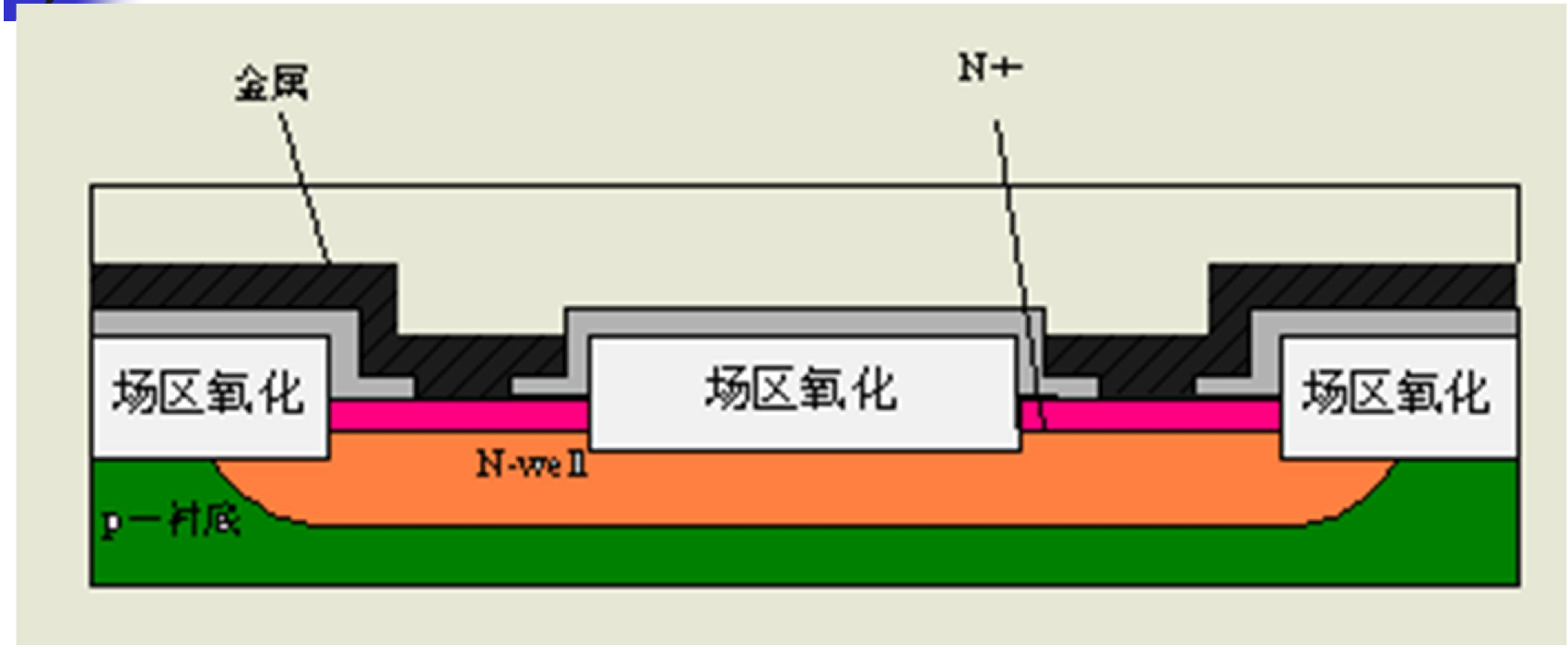
- **50－150Ω/方块**
- 存在对衬底的寄生电容

MOS工艺：多晶硅电阻



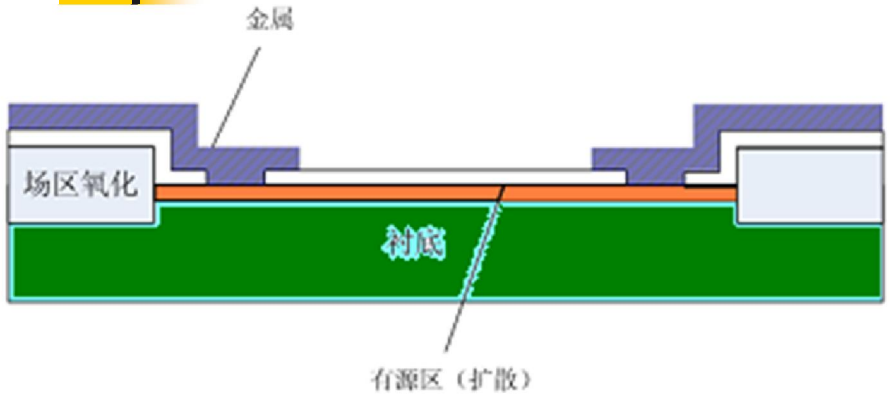
30－200Ω/方块

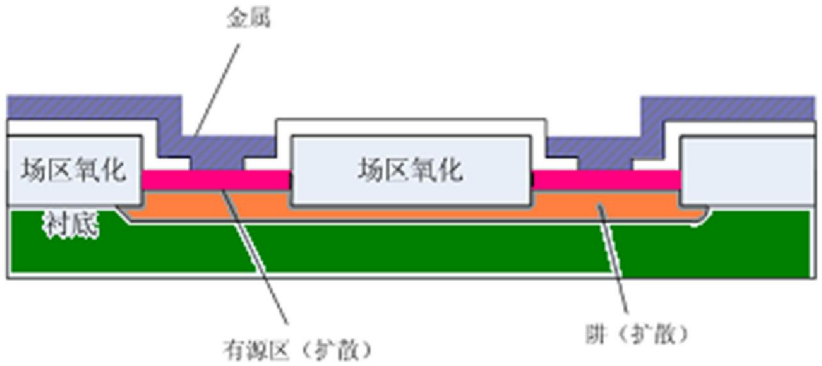
MOS工艺：阱电阻

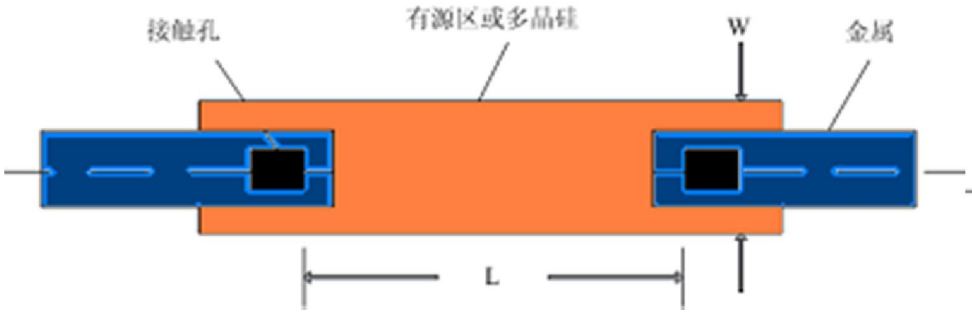


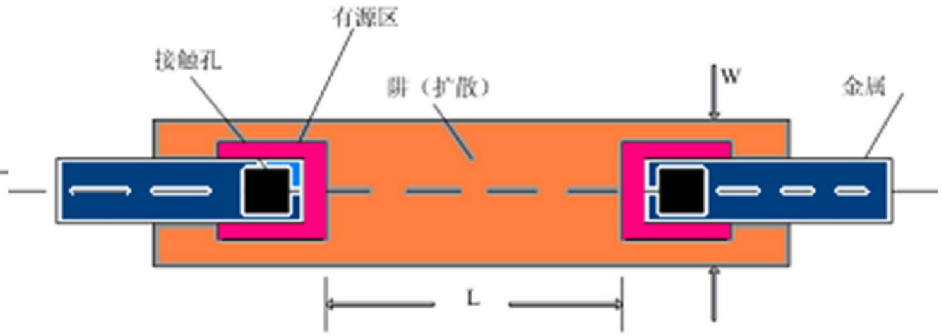
1－10kΩ/方块

电阻器的版图设计









$$R = \rho \frac{L}{TW} = R_{\square} \frac{L}{W}, \qquad R_{\square} = \frac{\rho}{T}$$

0.8μm CMOS工艺中电阻器的性能参数

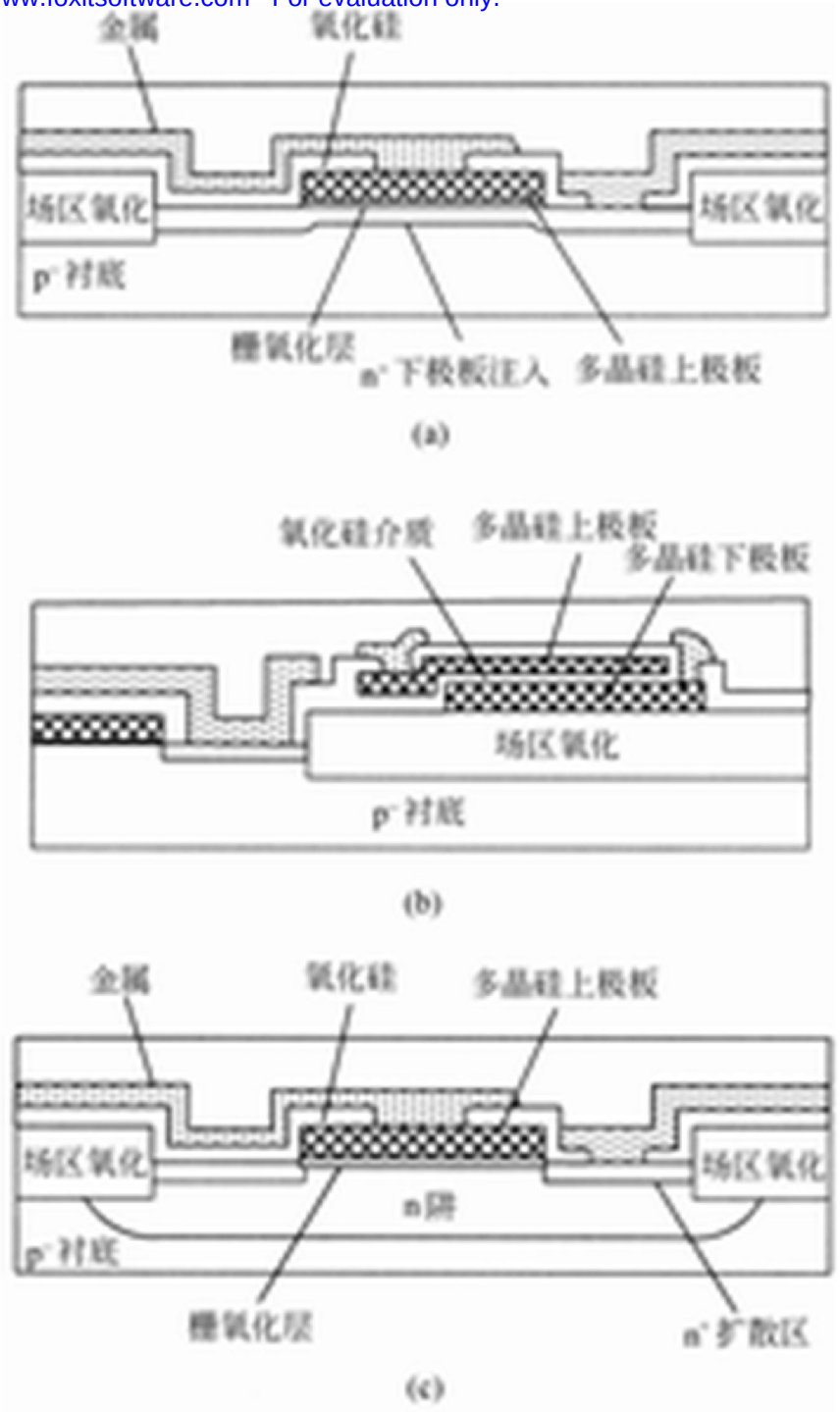
元件类型	数值范围 Ω/□	匹配精度 %	温度系数 10^{-6}/° C	电压系数 10^{-6} /V
p^+扩散电阻	80-150	0.4	1500	200
n^+扩散电阻	50-80	0.4	1500	200
Poly电阻	20-40	0.4	1500	100
n－well电阻	1-2k	—	8000	200

集成电路中的元器件

- 集成电阻器
- 集成电容器
- 集成电路中的互连线

几种电容结构

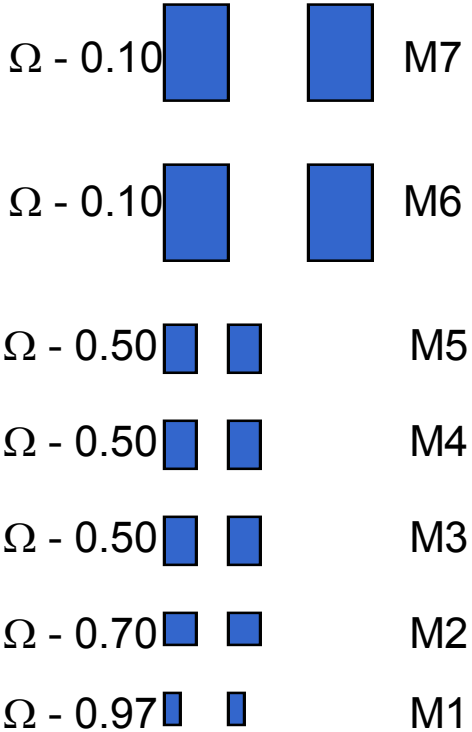
- **MOS**电容
- 双层多晶硅（金属）叠置电容
- 阱区**MOS**电容

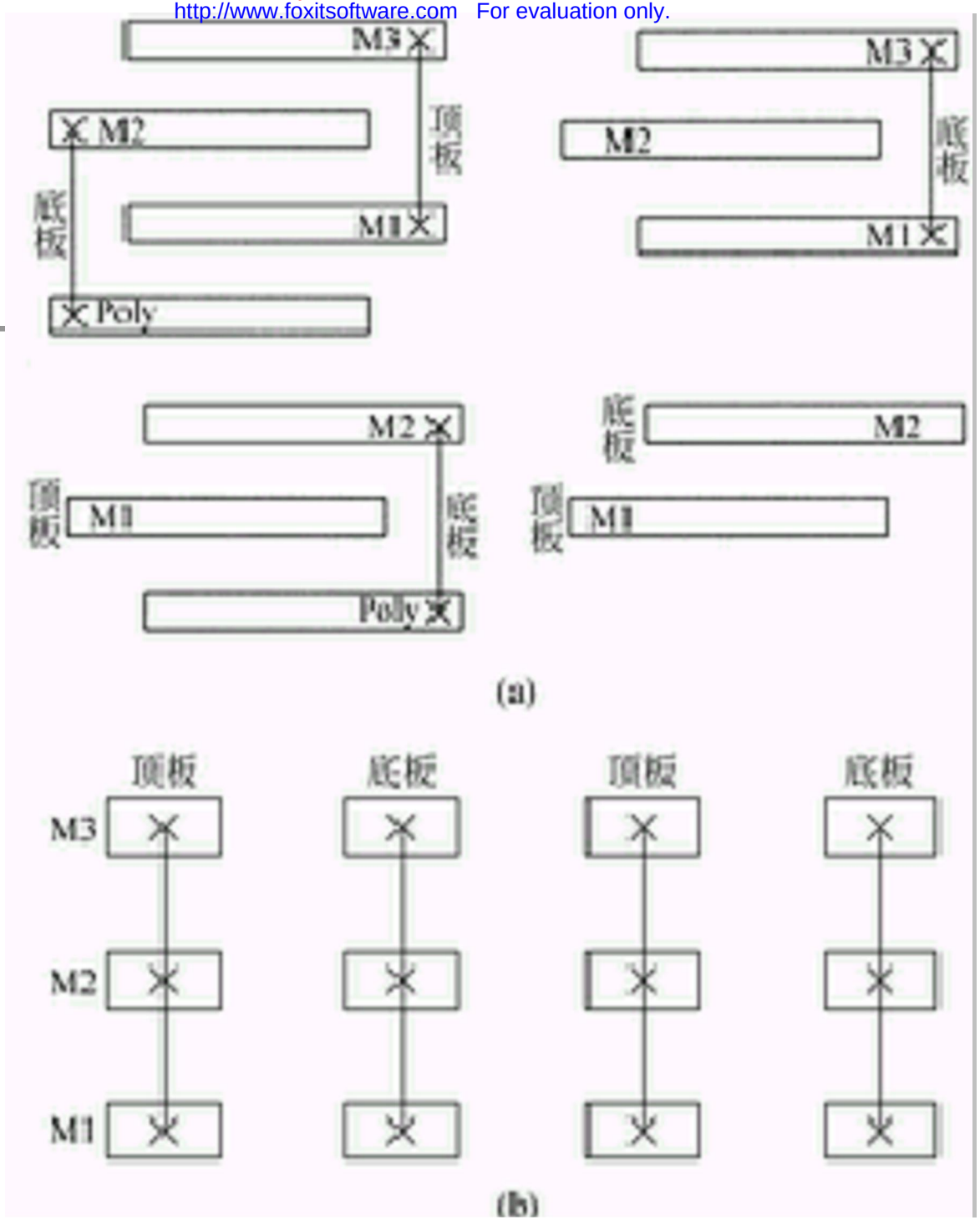


多层金属：

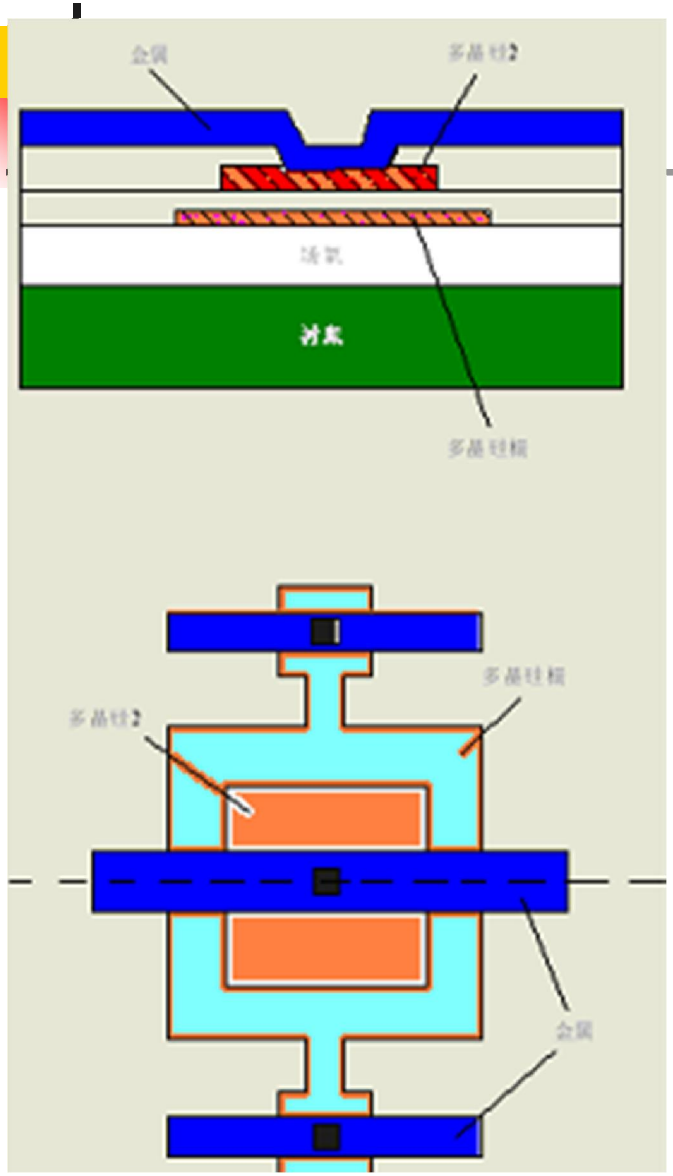
垂直电容

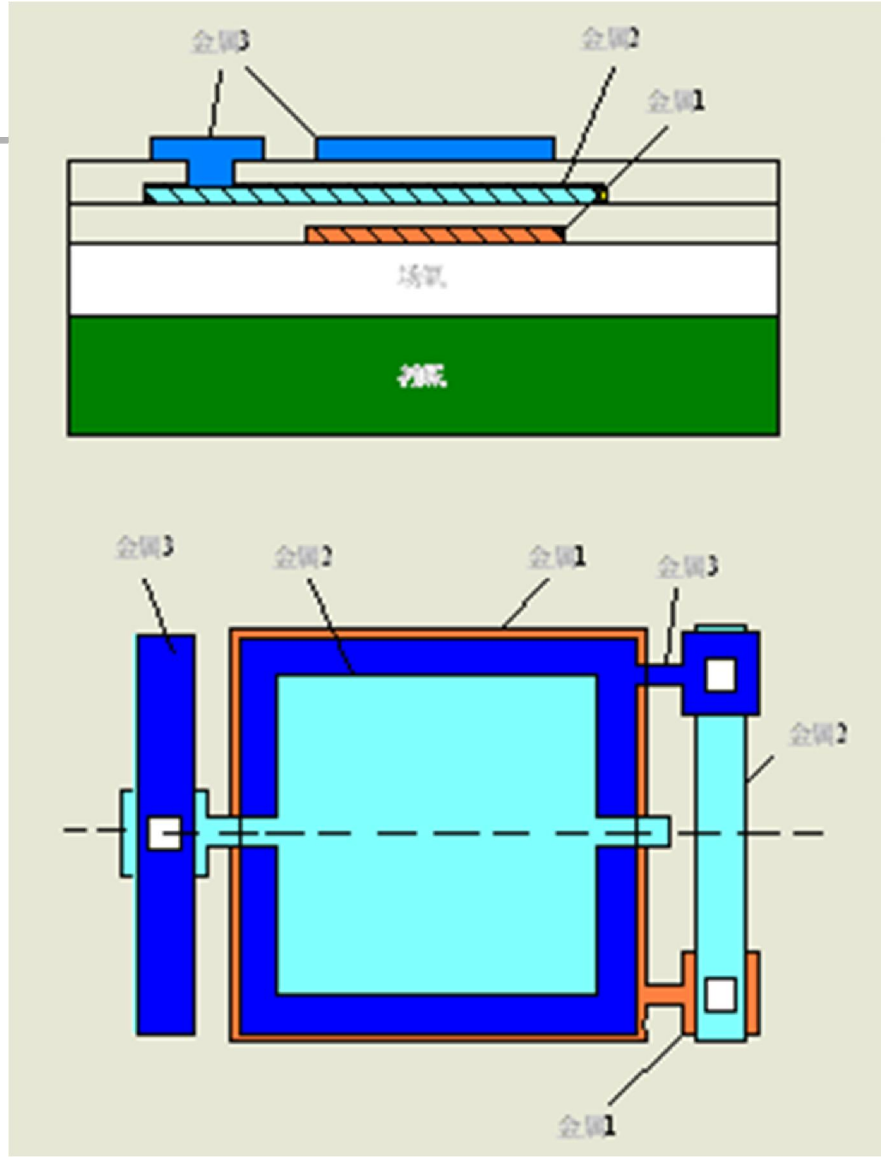
水平电容



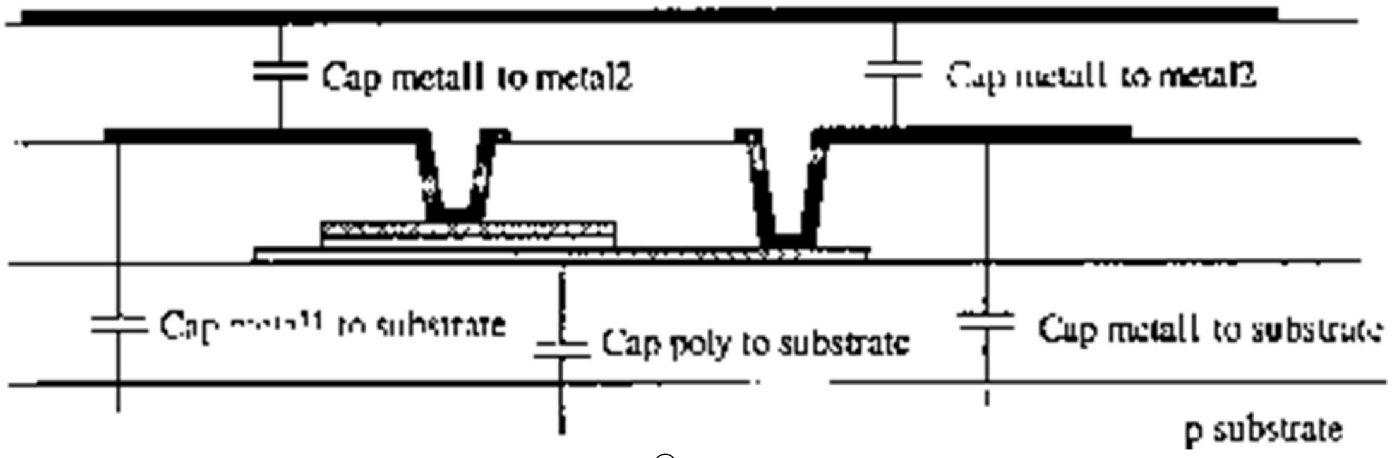


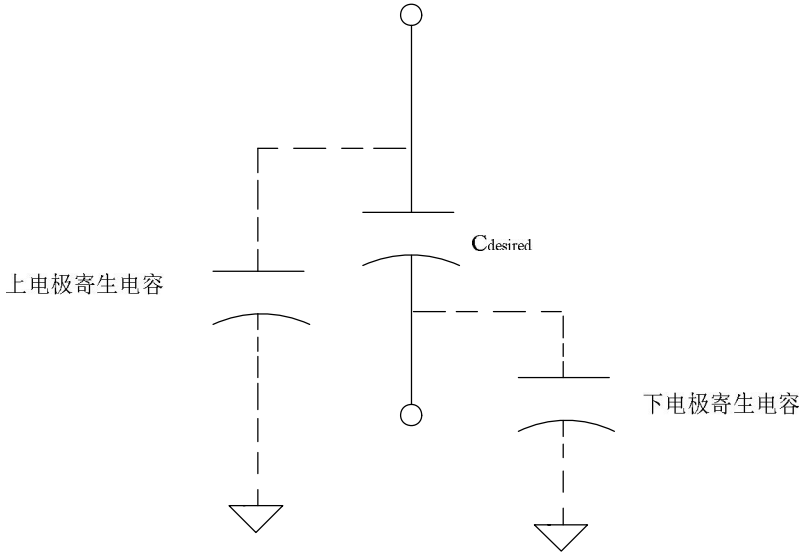
电容器的版图设计





电容器的寄生效应





0.8μm CMOS工艺中电容器的性能参数

元件类型	数值范围 $fF/\mu m^2$	匹配精度 %	温度系数 $10^{-6}/°C$	电压系数 $10^{-6}/V$
MOS电容	2.2-2.7	0.05	50	50
Poly/poly电容	0.8-1.0	0.05	50	50
M1－Poly电容	0.021-0.025	1.5	—	—
M2－M1电容	0.021-0.025	1.5	—	—
M3－M2电容	0.021-0.025	1.5	—	—

集成电路中的元器件

- 集成电阻器
- 集成电容器
- 集成电路中的互连线

连线寄生效应的影响

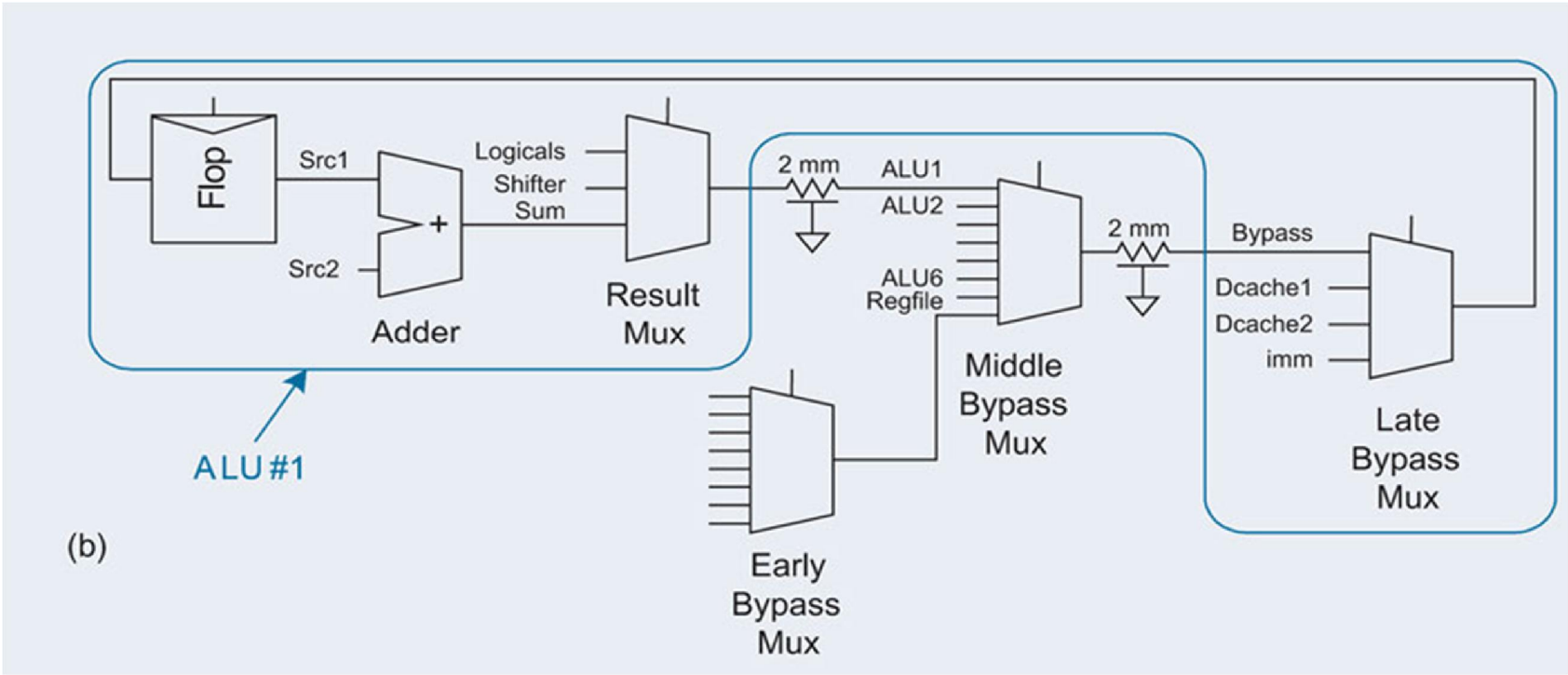
- 连线存在着寄生电阻、电容和电感
- 按比例缩小后电路连线的电阻增大
- 芯片面积增大使连线长度增加，连线**RC**延迟影响加大
- 连线寄生效应对电路可靠性和速度带来影响

连线按比例缩小后的性质

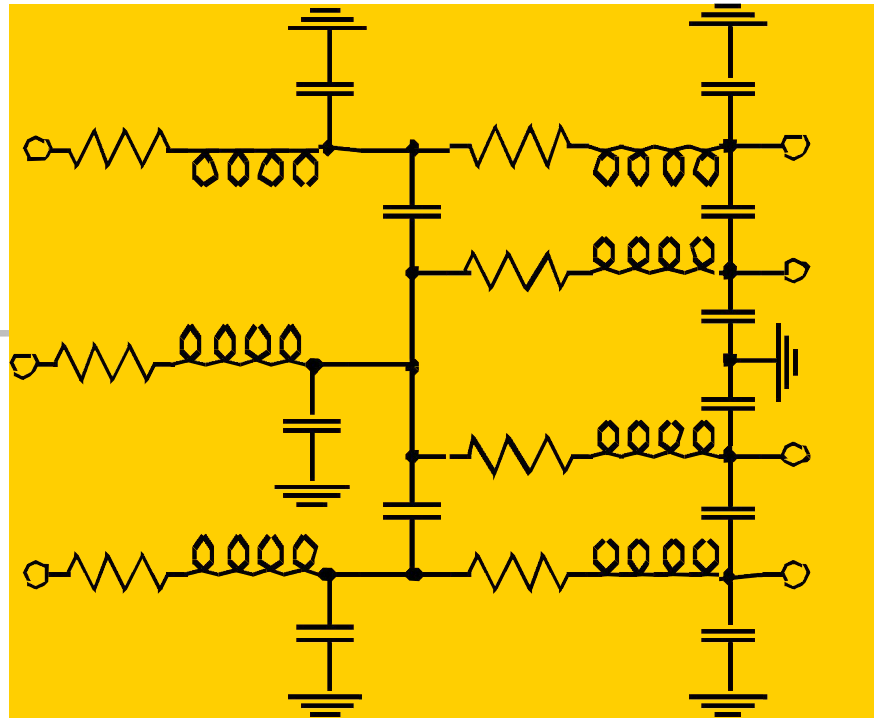
连线参数	比例因子 (CR)	比例因子 (CV)
几何尺寸 L, W, H, Ls, Xox	1/k	1/k
电阻 R = ρ*L/WH	k	k
电容 Cox, C_F	1/k	1/k
延迟时间 0.85*RC	1	1
电压降 IR	1	k^2
电流密度 I/WH	k	k^3
接触孔电阻	k^2	k^2
接触孔电压降	k	k^3

模块	最大延迟时间(ps)
Adder	600
Result Mux	60
Early Bypass Mux	100
Middle Bypass Mux	80
Late Bypass Mux	75
2mm wire	100

- Itanium处理器的算术逻辑单元的结构图,如果触发器的建立时间为65ps,clk到输出Q的延迟时间为50ps,而其他组合逻辑的延迟时间如表1中所示.

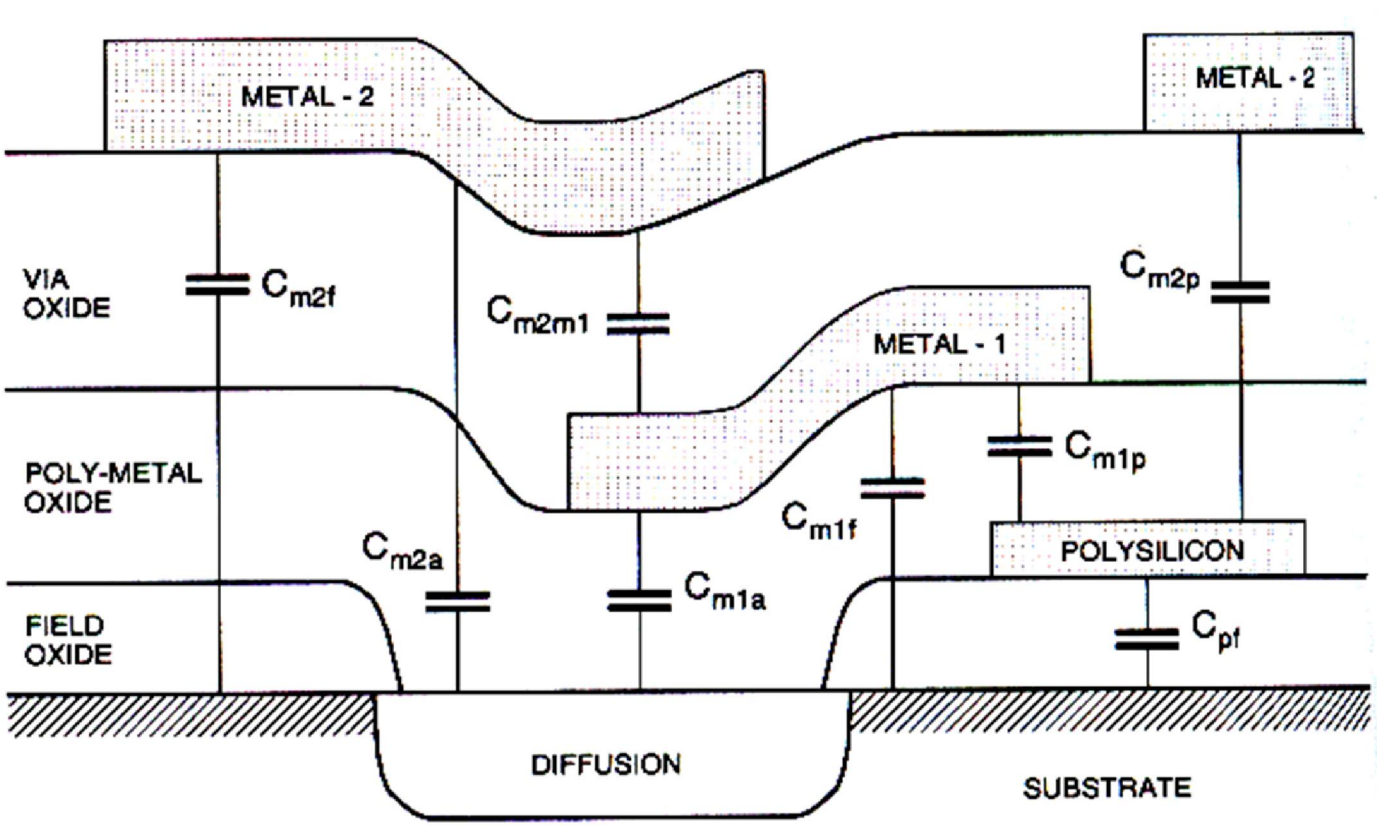


互连线

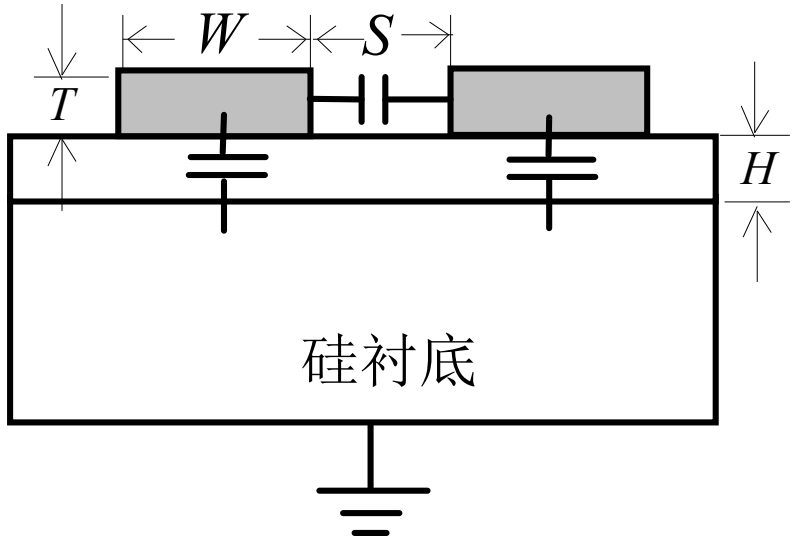


- 寄生电容
- 寄生电阻
- 寄生电感
- 互连线引起的可靠性问题
- 互连线的**RC**延迟

连线的寄生电容



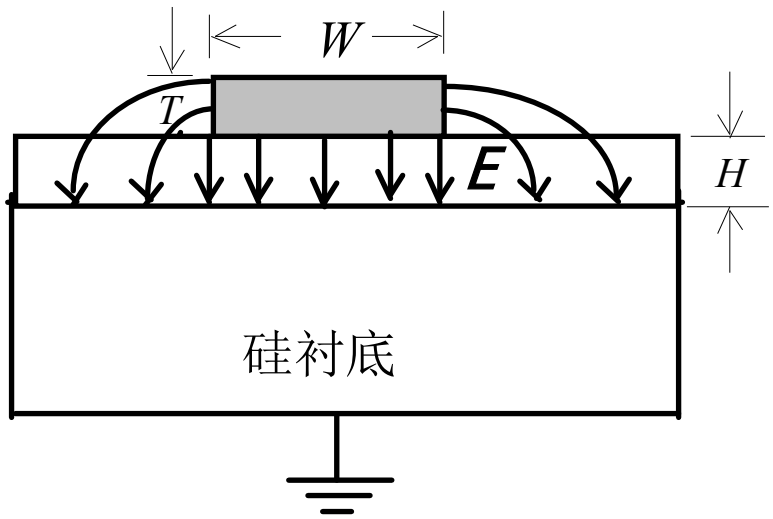
互连线电容

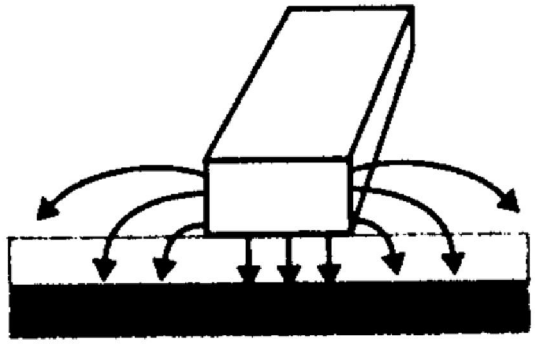


$$C_{\mathrm{v}} = \frac{\varepsilon_0 \varepsilon_{ox}}{H} WL,\ C_{\mathrm{m}} = \frac{\varepsilon_0 \varepsilon_{ox}}{S} TL$$

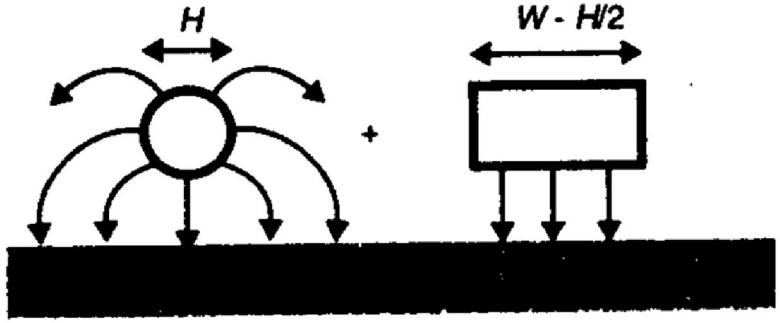
$$C_{\mathrm{l}} \approx k\left(C_{\mathrm{v}} + 2C_{\mathrm{m}}\right)$$

边缘效应





(a) Fringing fields

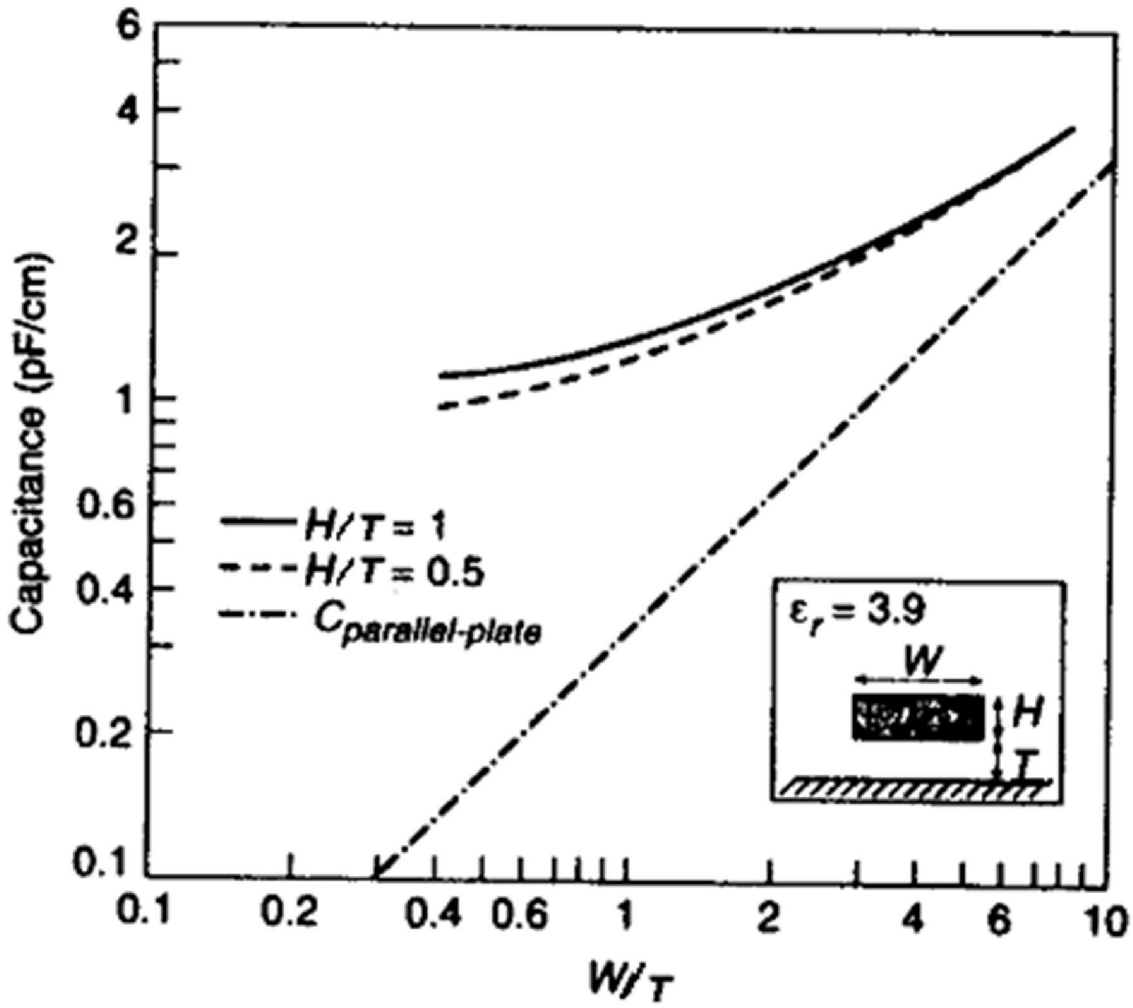


(b) Model of fringing field capacitance.

$$C_{\mathrm{v}} = \frac{\varepsilon_0 \varepsilon_{ox}}{H} WL$$

$$C_V = \varepsilon_0 \varepsilon_{ox} L \left[\left(\frac{W - H/2}{t_{ox}} \right) + \left(\frac{2\pi}{\log(t_{ox}/H)} \right) \right]$$

边缘效应对互连线电容影响

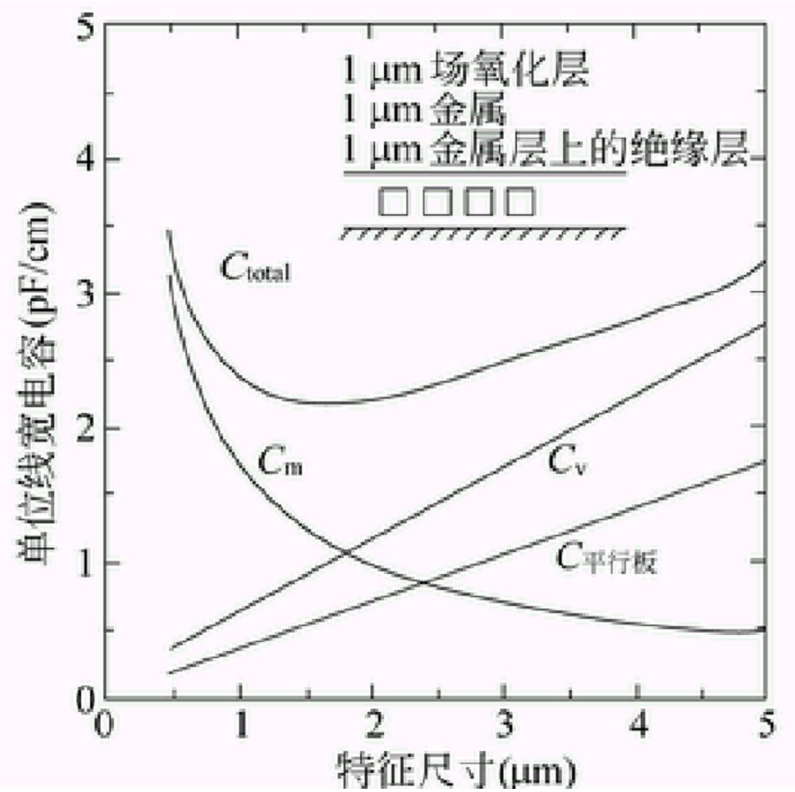


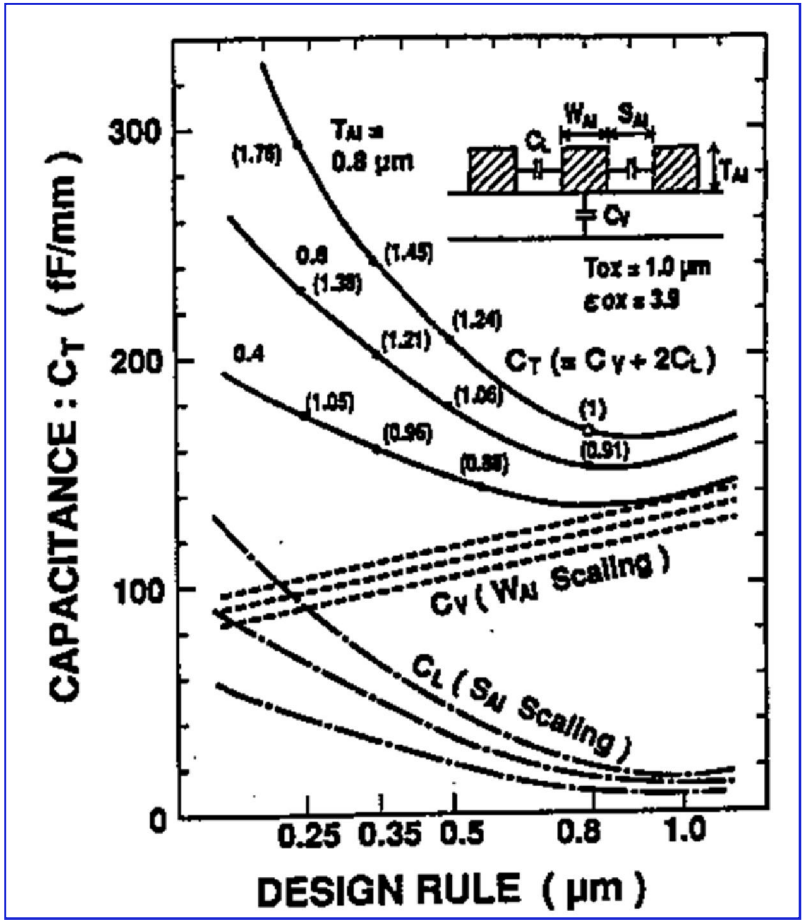
连线寄生电容典型值

元件类型	数值范围 $fF/\mu m^2$	匹配精度 %	温度系数 $10^{-6}/°C$	电压系数 $10^{-6}/V$
MOS电容	2.2-2.7	0.05	50	50
Poly/poly电容	0.8-1.0	0.05	50	50
M1－Poly电容	0.021-0.025	1.5	—	—
M2－M1电容	0.021-0.025	1.5	—	—
M3－M2电容	0.021-0.025	1.5	—	—

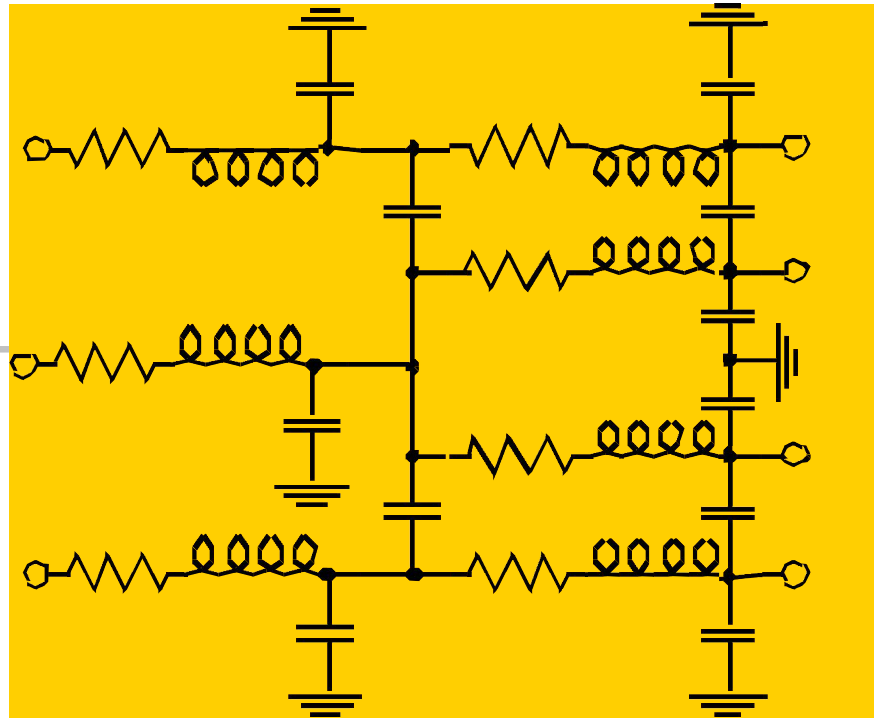
电容类型	单位面积电容（$fF/\mu m^2$）	单位周长电容（$fF/\mu m$）
金属1-衬底	0.030	0.044
多晶硅-衬底	0.066	0.046
金属2-衬底	0.016	0.042
金属1-多晶硅	0.053	0.051
金属2-多晶硅	0.021	0.045
金属2-金属1	0.035	0.051

互连线寄生电容：特征尺寸减小





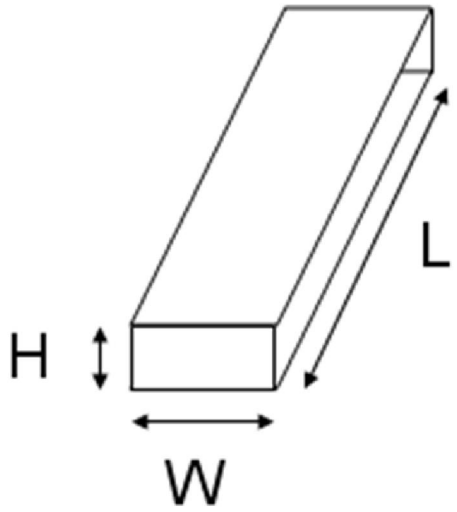
互连线



- 寄生电容
- 寄生电阻
- 寄生电感
- 互连线引起的可靠性问题
- 互连线的**RC**延迟

连线的寄生电阻

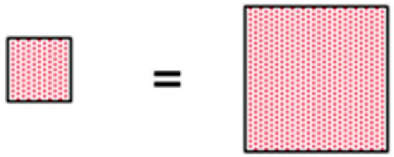
Wire Resistance



$$R = \frac{\rho L}{A} = \frac{\rho}{H}\frac{L}{W}$$

Sheet Resistance $R_{\square}$

$R_{1\square} = R_{2\square}$



不同连线材料的电阻率

材料	电阻率(Ω-m)
银(Ag)	1.6×10^{-8}
铜(Cu)	1.7×10^{-8}
金(Au)	2.2×10^{-8}
铝(Al)	2.7×10^{-8}
钨(W)	5.5×10^{-8}

不同材料的方块电阻

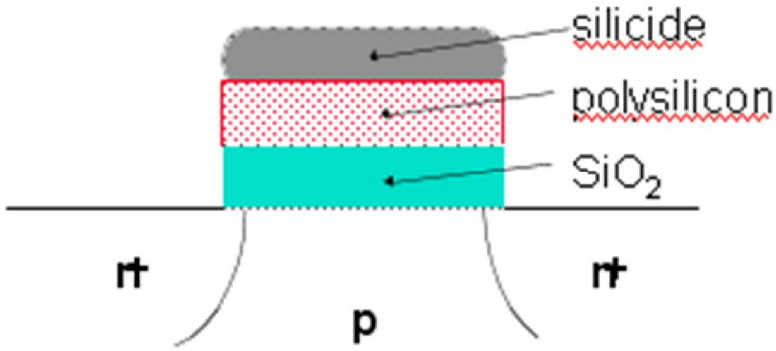
(针对0.25umCMOS工艺)

材料	方块电阻(Ω/□)
n+、 p+扩散层	50~150
n+、 p+扩散层 （有硅化物 ）	3~5
N阱	1000 ~1500
多晶硅	150~200
多晶硅（有硅化物 ）	4~5
金属铝	0.05~0.1

减小互连线寄生电阻

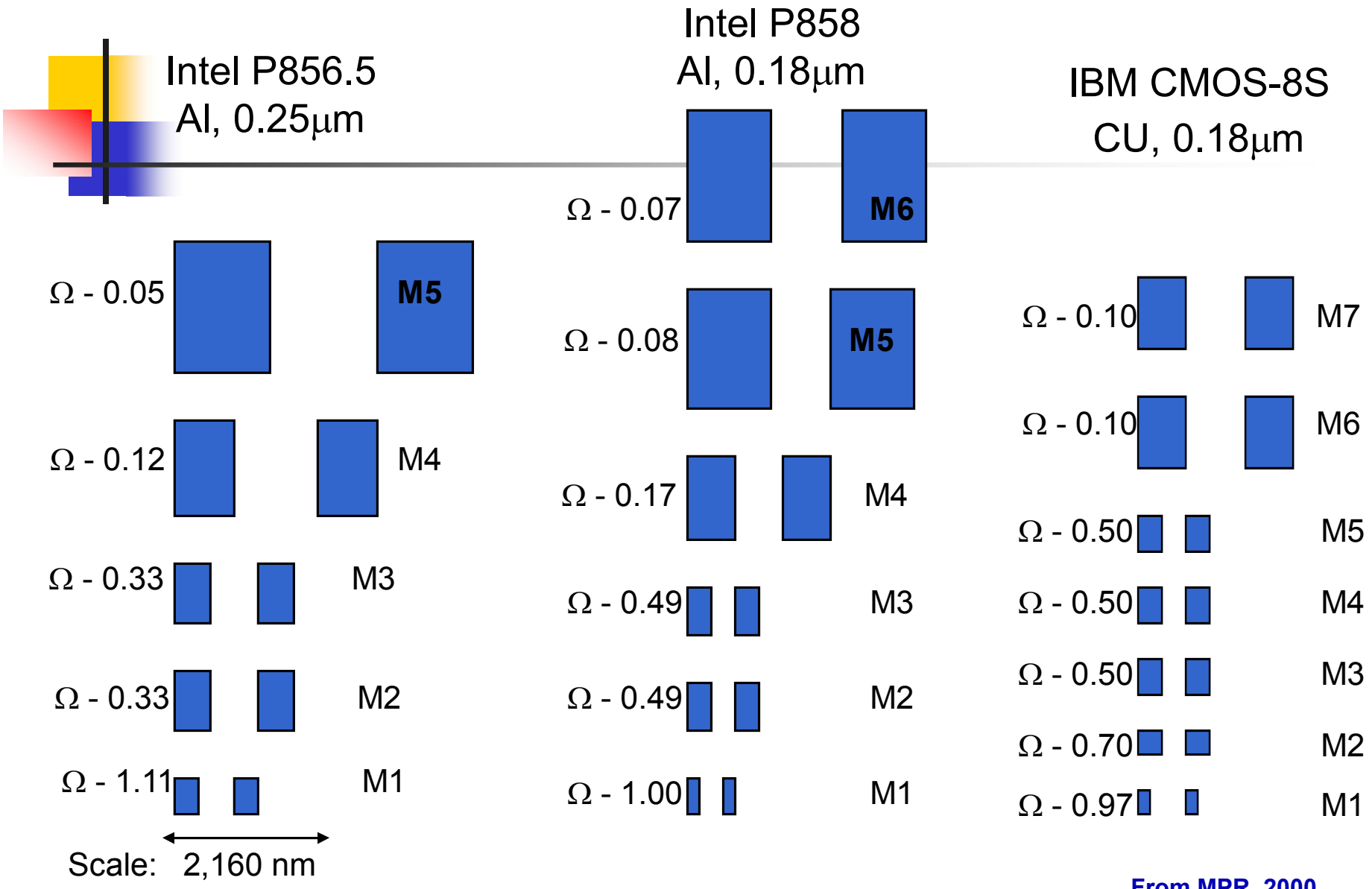
Overcoming Interconnect Resistance

- Selective technology scaling
  - scale W while holding H constant
- Use better interconnect materials
  - lower resistivity materials like copper
  - use silicides (WSi_2, $TiSi_2$, $PtSi_2$ and TaSi)
    - Conductivity is 8-10 times better than poly alone



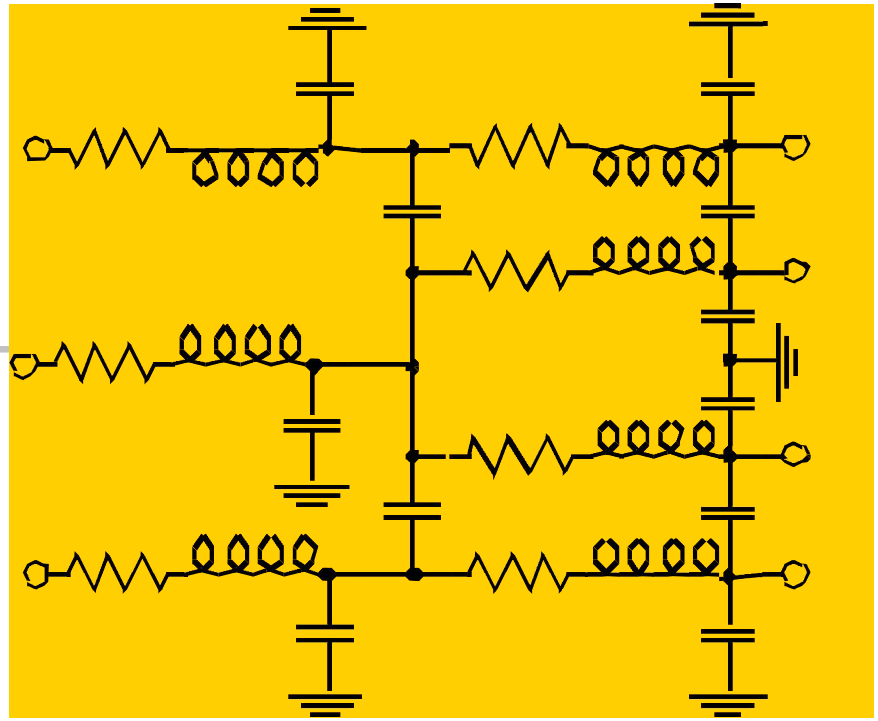
- Use more interconnect layers
  - reduces the average wire length L (but beware of extra contacts)

Wire Spacing Comparisons



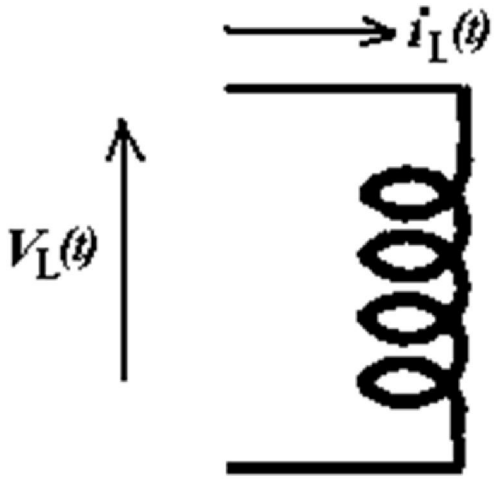
From MPR, 2000

互连线



- 寄生电容
- 寄生电阻
- 寄生电感
- 互连线引起的可靠性问题
- 互连线的**RC**延迟

连线的寄生电感



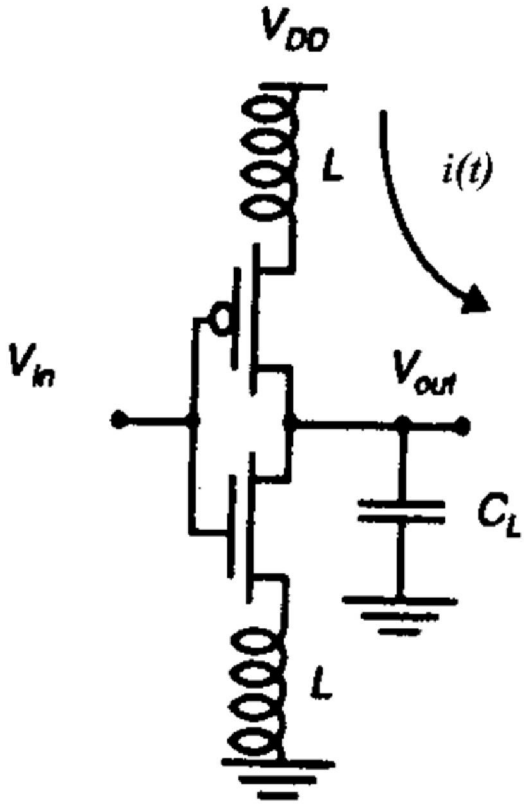
$$V_L(t) = L\frac{\mathrm{d}i_L}{\mathrm{d}t}$$

寄生电感的典型值

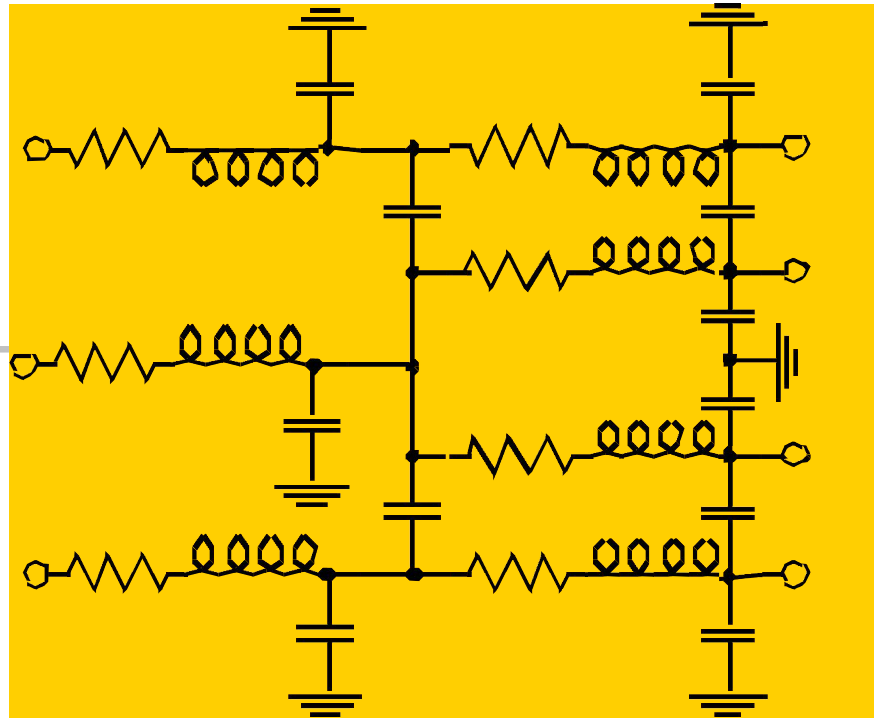
封装引脚和键合线的寄生电容和电感

封装类型	电容 (pF)	电感(nH)
68-pin plastic DIP	4	35
68-pin ceramic DIP	7	20
256-pin grid array	1-5	2-15
键合线	0.5-1	1-2
压焊块	0.1-0.5	0.01-0.1

电感对输出电压的影响



互连线



- 寄生电容
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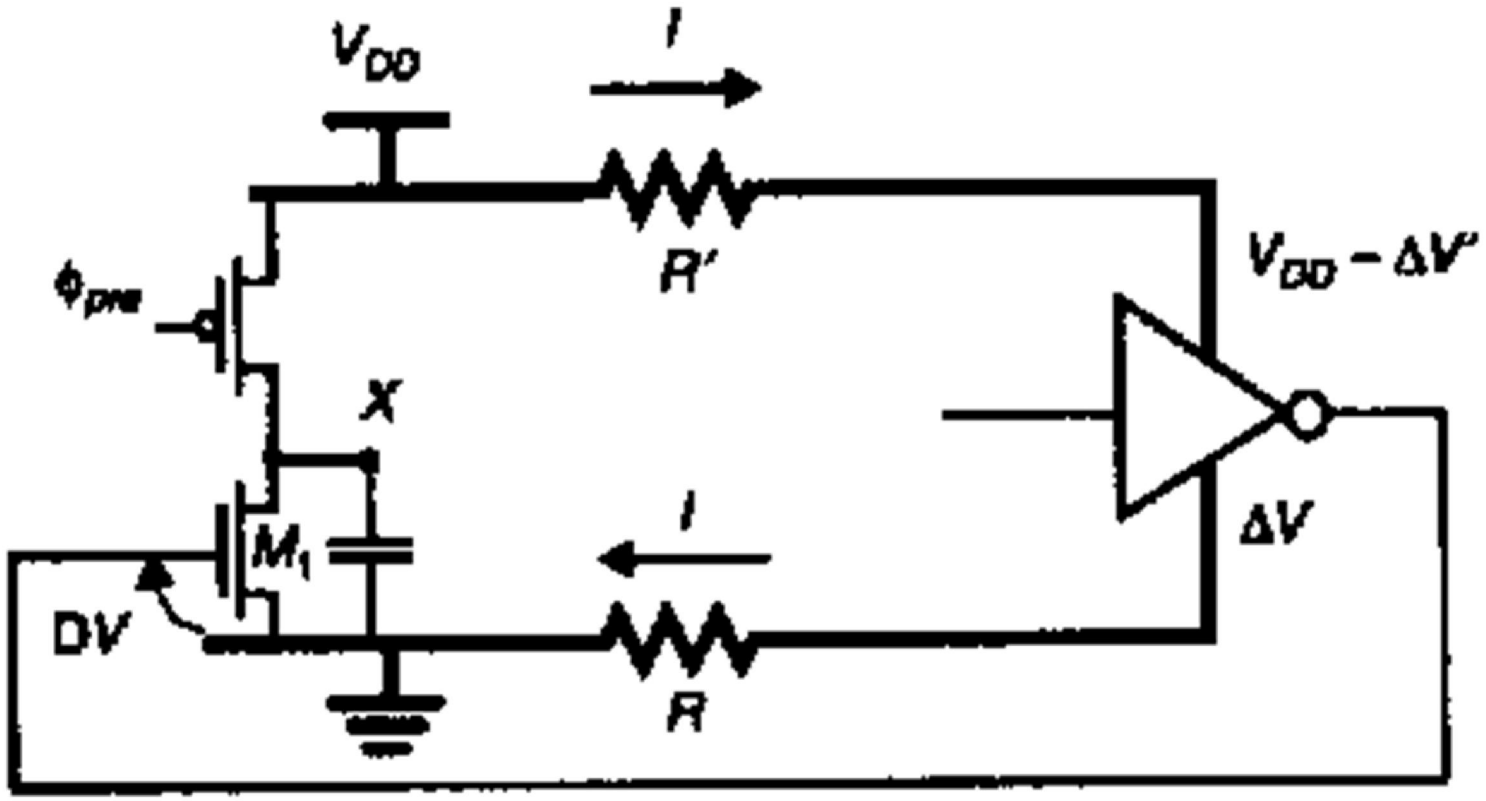
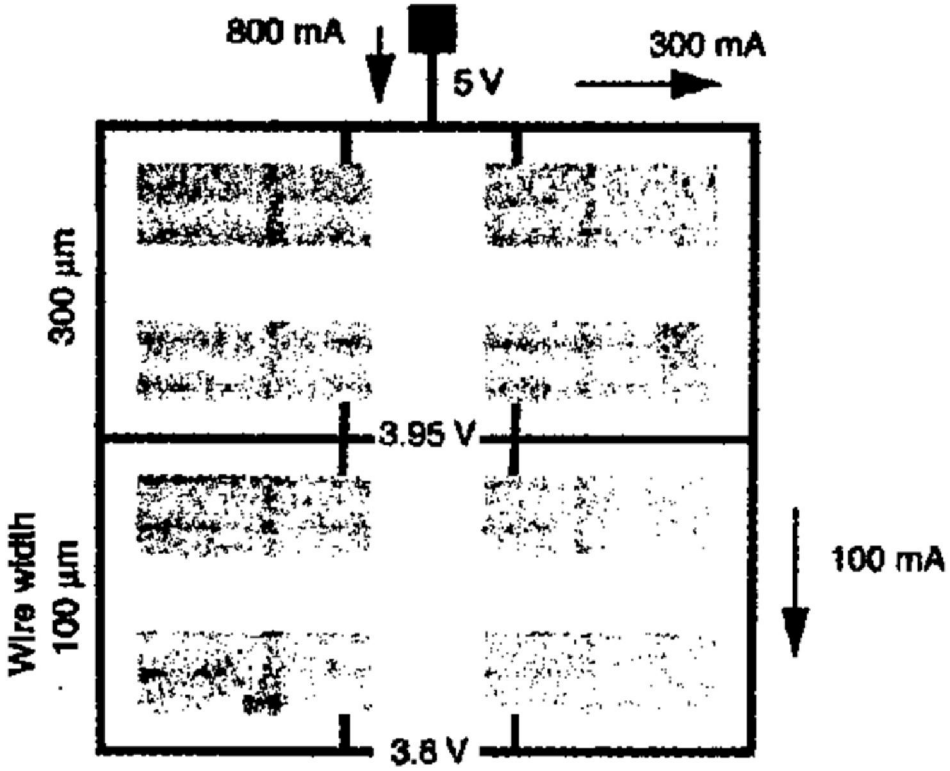
- 互连线引起的可靠性问题
- 互连线的**RC**延迟

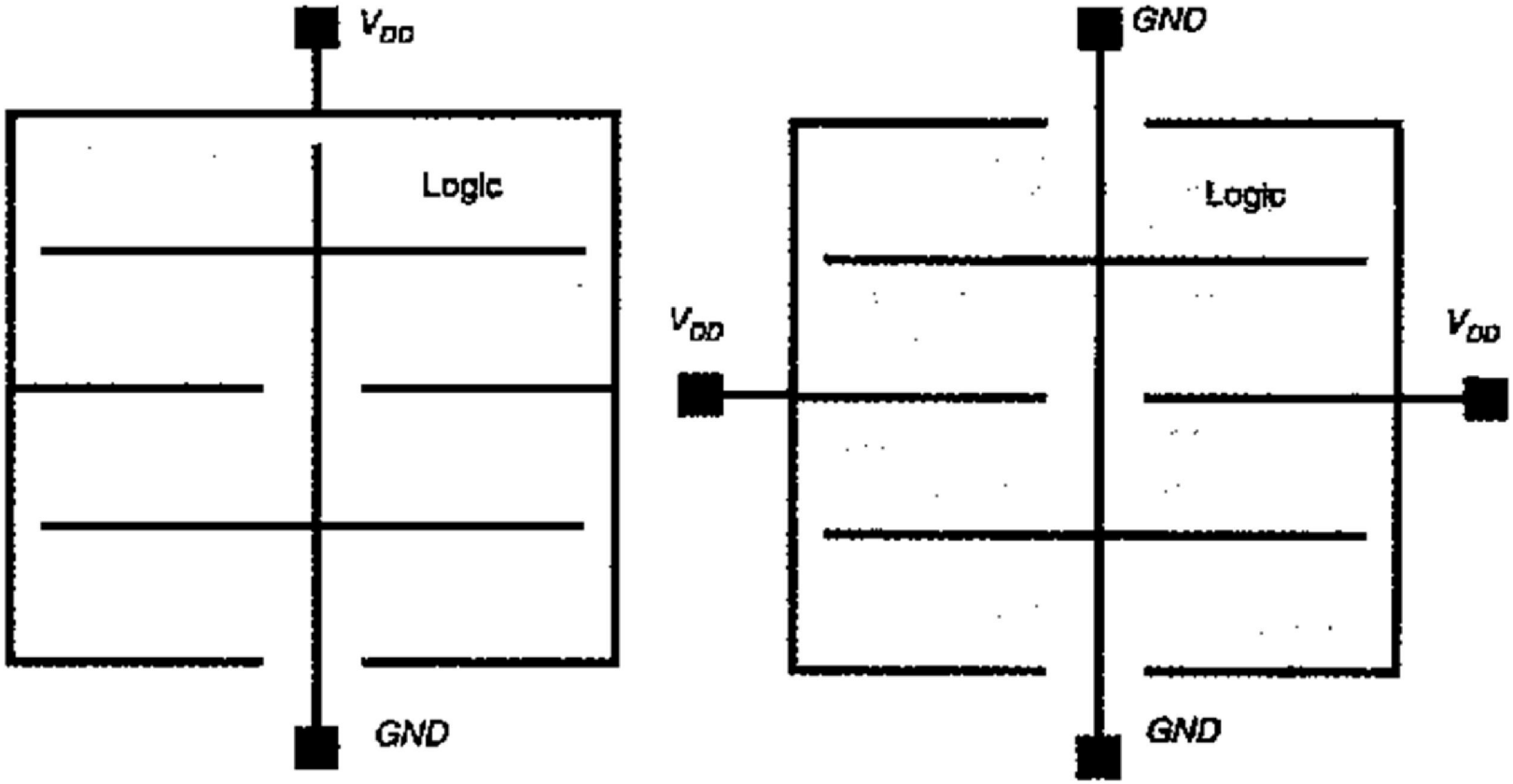
连线寄生电阻：欧姆压降（IR Drop）



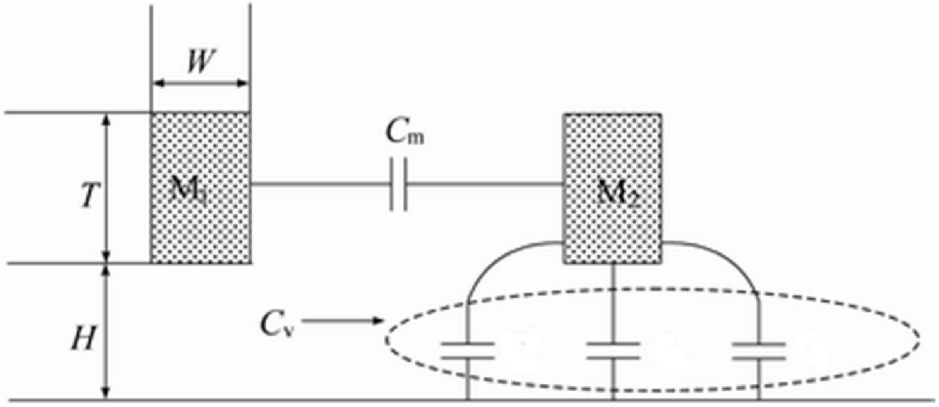
峰值电流在电源线上的压降



合理的电源线分布



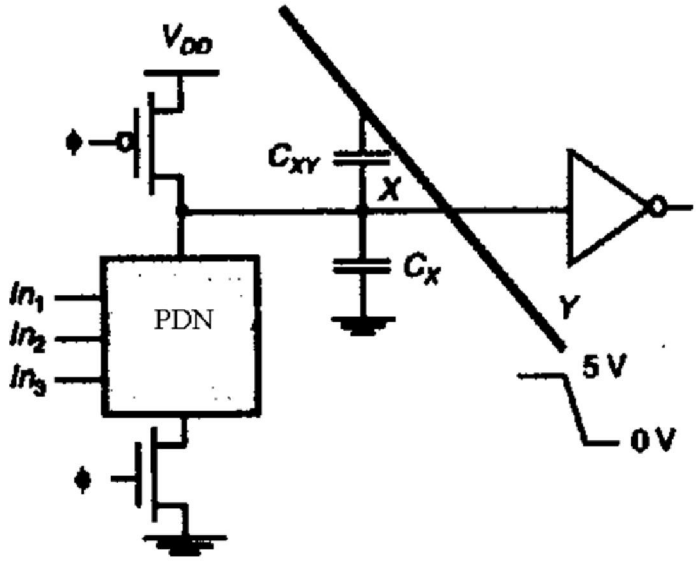
互连线寄生电容：线间串话

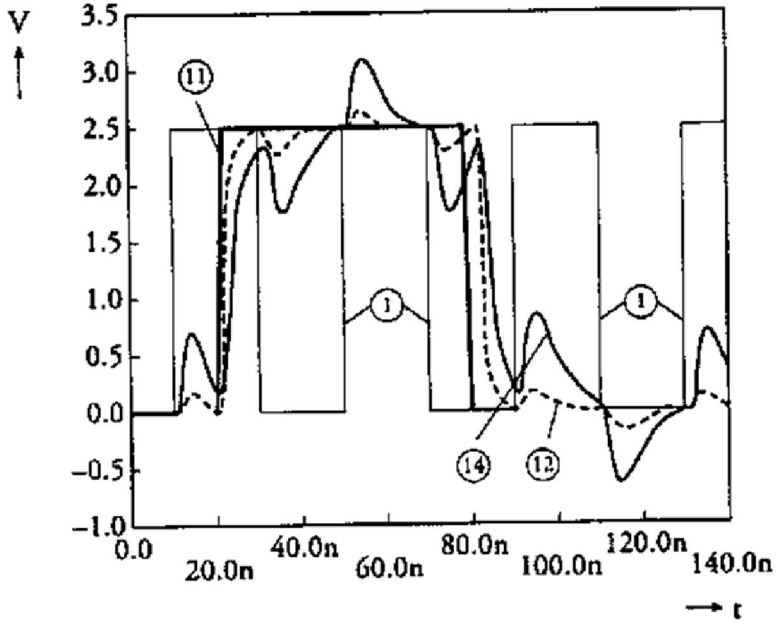


$$\Delta V_{\mathrm{M2}} = \frac{C_{\mathrm{m}}}{C_{\mathrm{m}} + C_{\mathrm{V}}} \Delta V_{\mathrm{M1}}$$

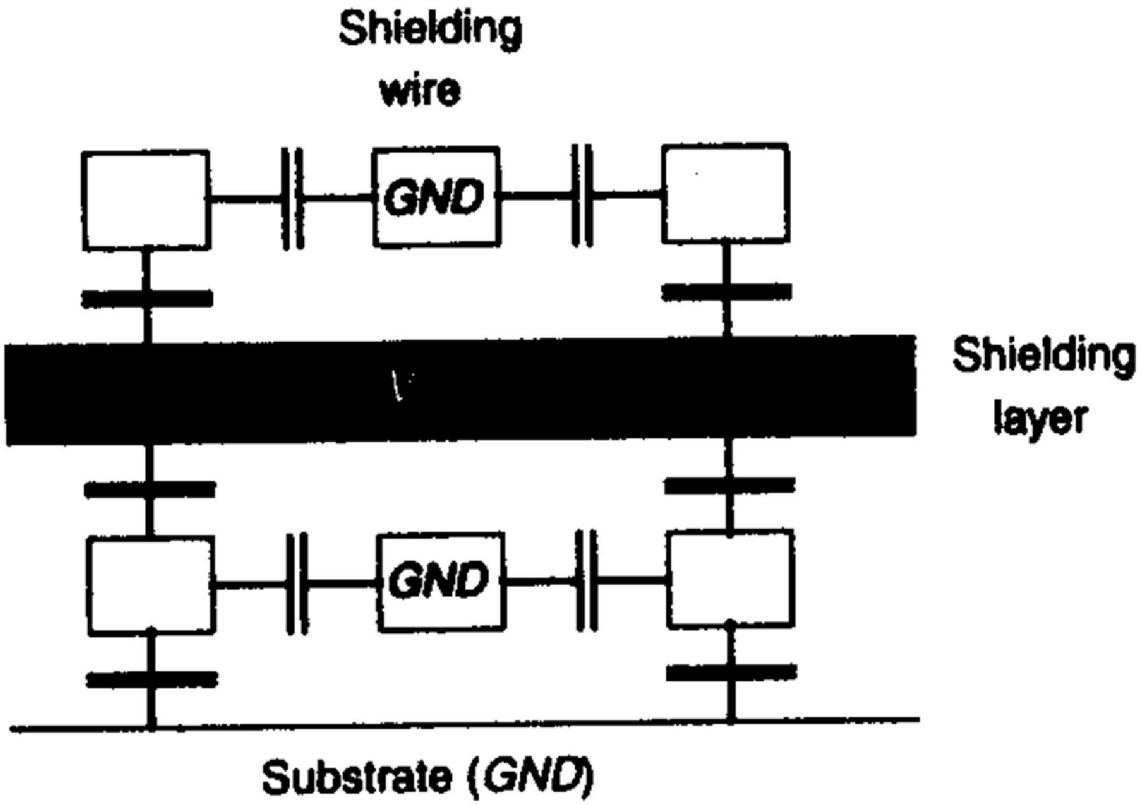
$$\Delta V_{\mathrm{M2}} = \frac{80}{80+40} \times 2.5 = 1.67(\mathrm{V})$$

线间串话对电路影响

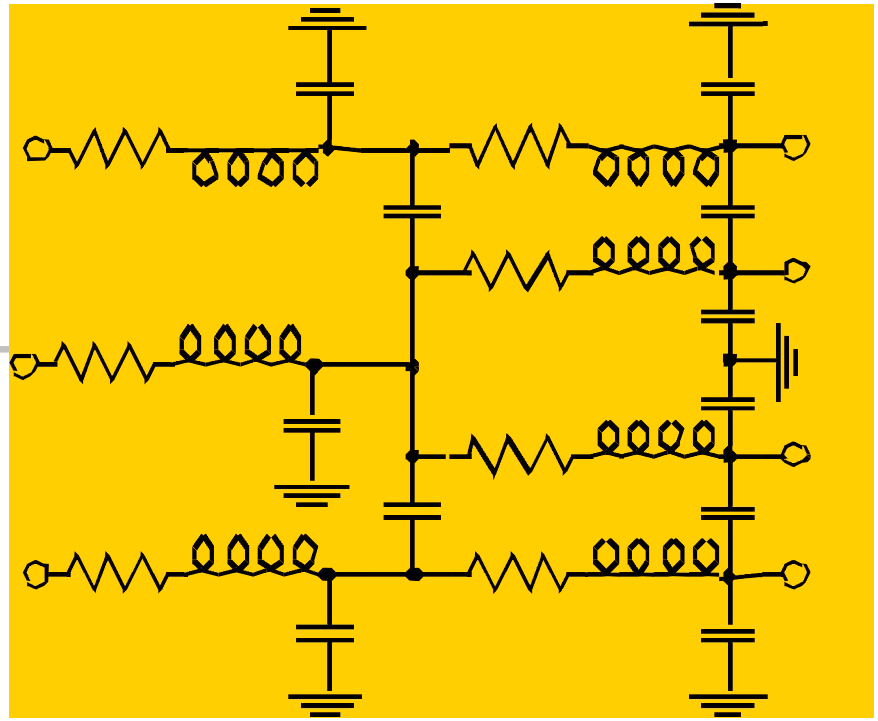




避免Cross Talk的措施

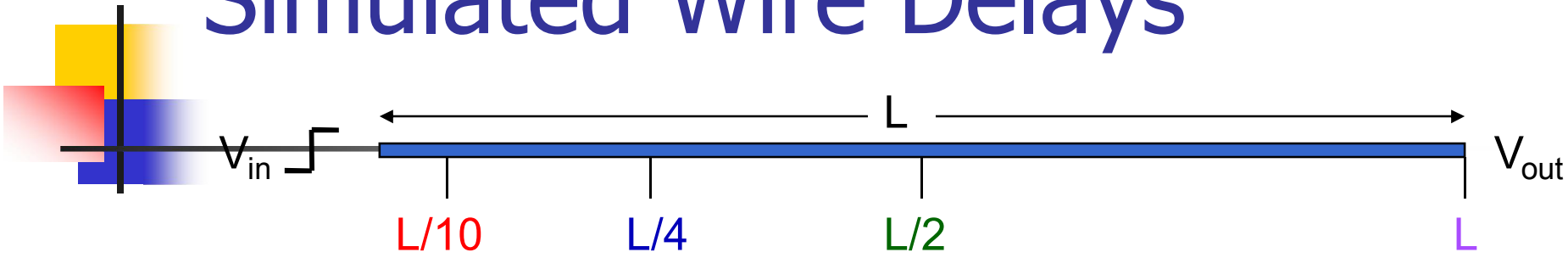


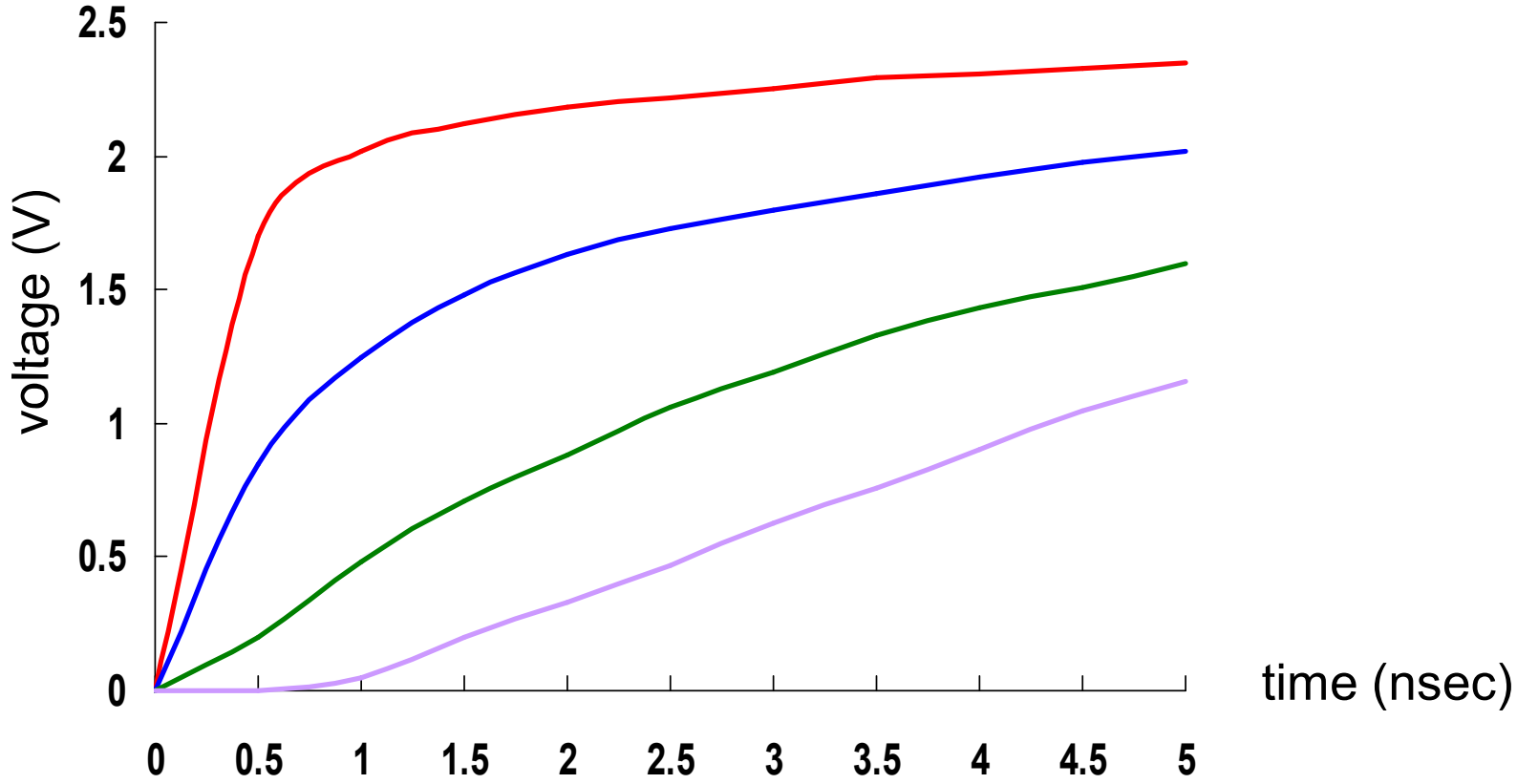
互连线



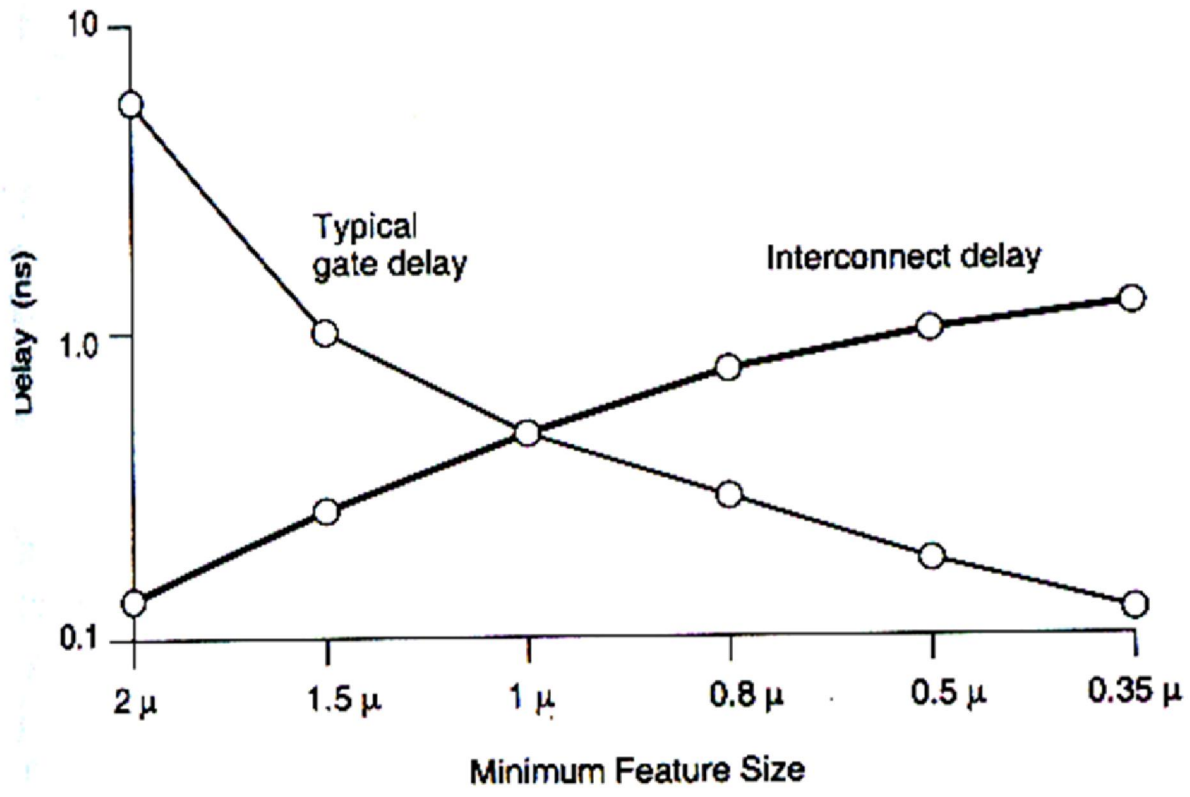
- 寄生电容
- 寄生电阻
- 寄生电感
- 互连线引起的可靠性问题
- 互连线的**RC**延迟

Simulated Wire Delays

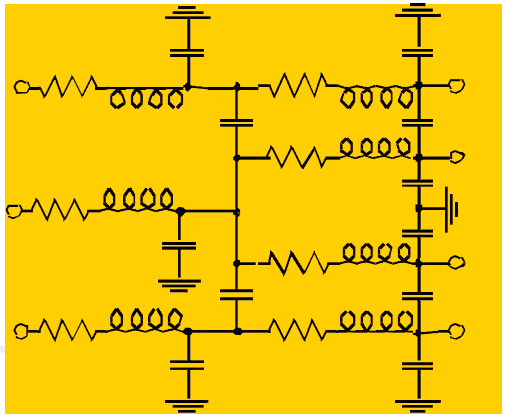


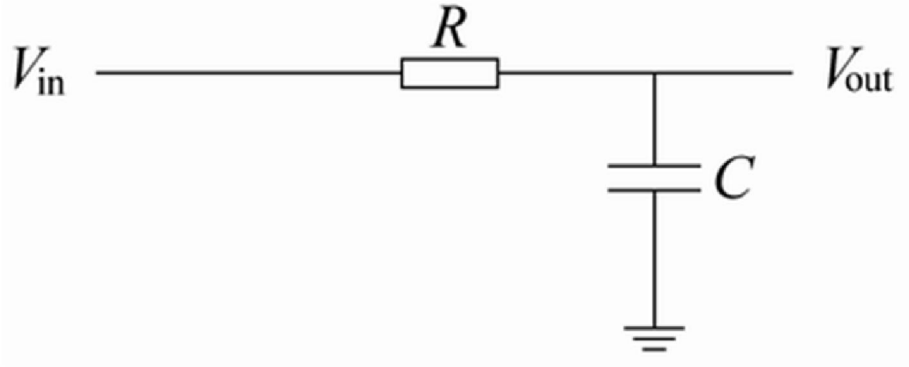


互连线延迟限制了电路速度提高



互连线RC延迟的集总模型





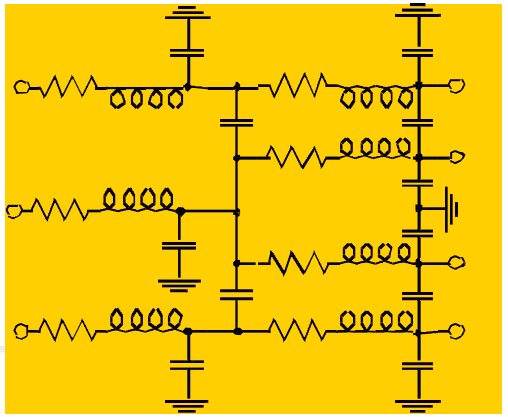
$$C_l \frac{\mathrm{d}V_{out}}{\mathrm{d}t} = \frac{V_{in} - V_{out}}{R_l}$$

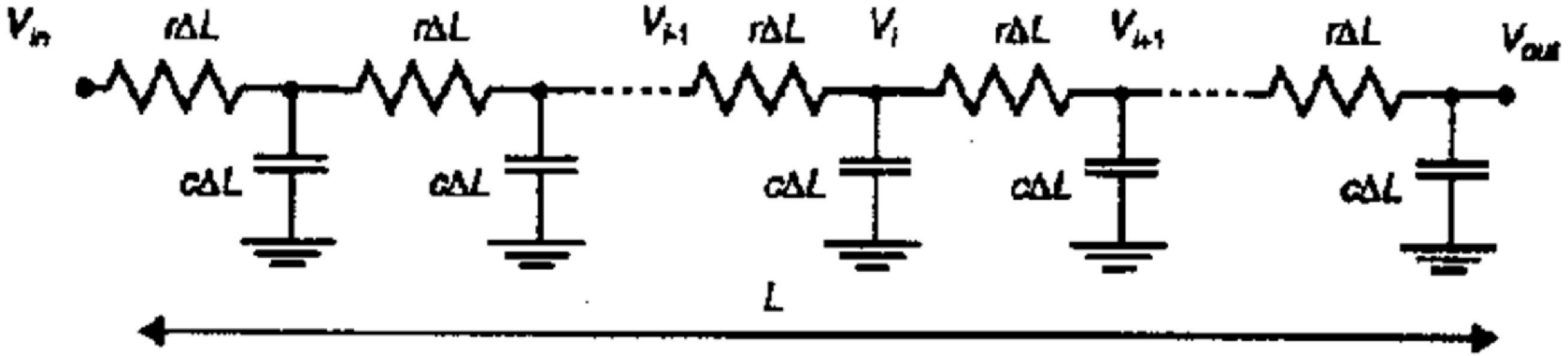
$$V_{out}(t) = \left(1 - \mathrm{e}^{-t/\tau}\right) V_{DD}, \qquad \tau = R_l C_l$$

$$V_{out} = 50\% V_{DD} \qquad t = 0.69\tau$$

$$V_{out} = 90\% V_{DD} \qquad t = 2.2\tau$$

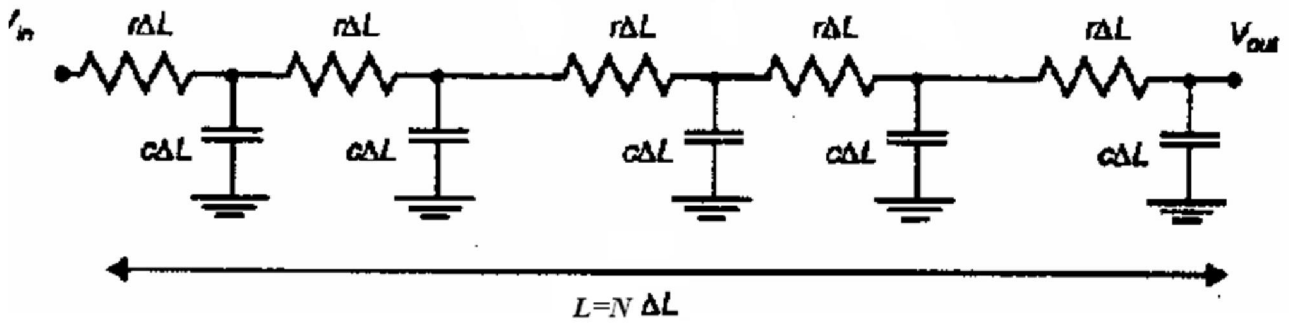
连线RC延迟的分布模型





$$c\Delta L\frac{\partial V_i}{\partial t}=\frac{(V_{i+1}-V_i)+(V_{i-1}-V_i)}{r\Delta L}$$

连线RC延迟的分段集总模型



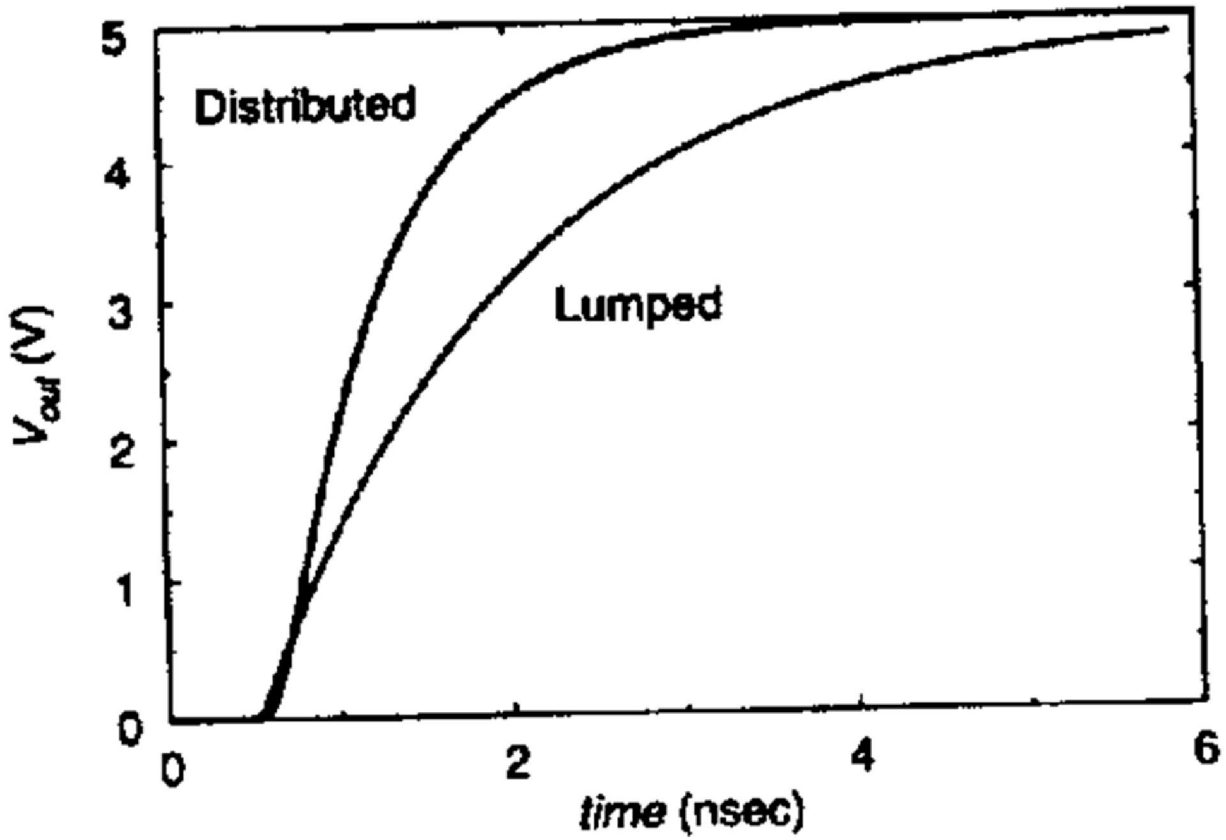
$$\tau(V_{out}) = (\Delta L)^2 (rc + 2rc + \cdots + Nrc), \qquad \Delta L = L/N$$

$$\tau(V_{out}) = rc(\Delta L)^2 \left[\frac{N(N+1)}{2}\right] = \frac{rcL^2}{2} = \frac{RC}{2}$$

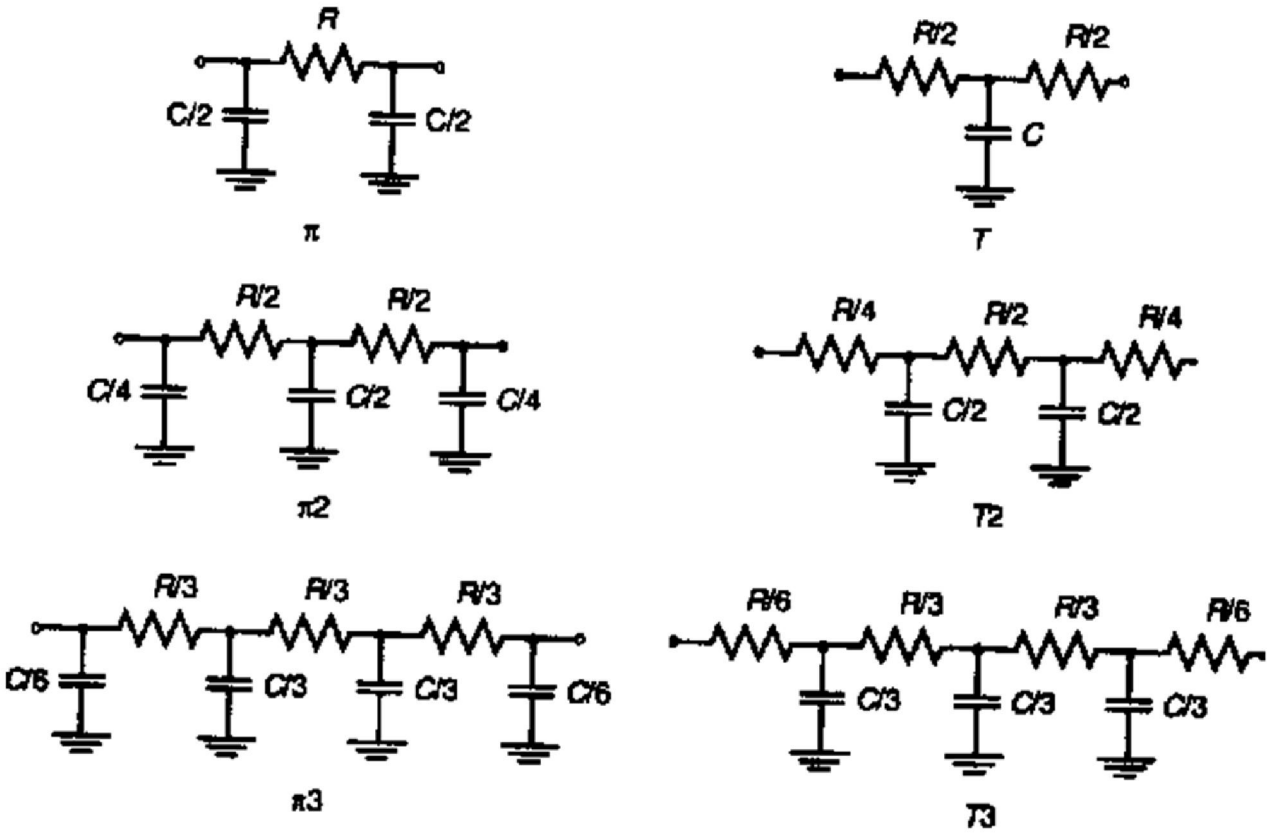
分布RC模型与集总RC模型的差别

电压变化范围	集总RC模型	分布RC模型
$0 \sim 50\%\ (t_{pd})$	$0.69RC$	$0.38\ RC$
$0 \sim 63\%\ (\tau)$	RC	$0.5\ RC$
$10\% \sim 90\%\ (t_r)$	$2.2\ RC$	$0.89\ RC$

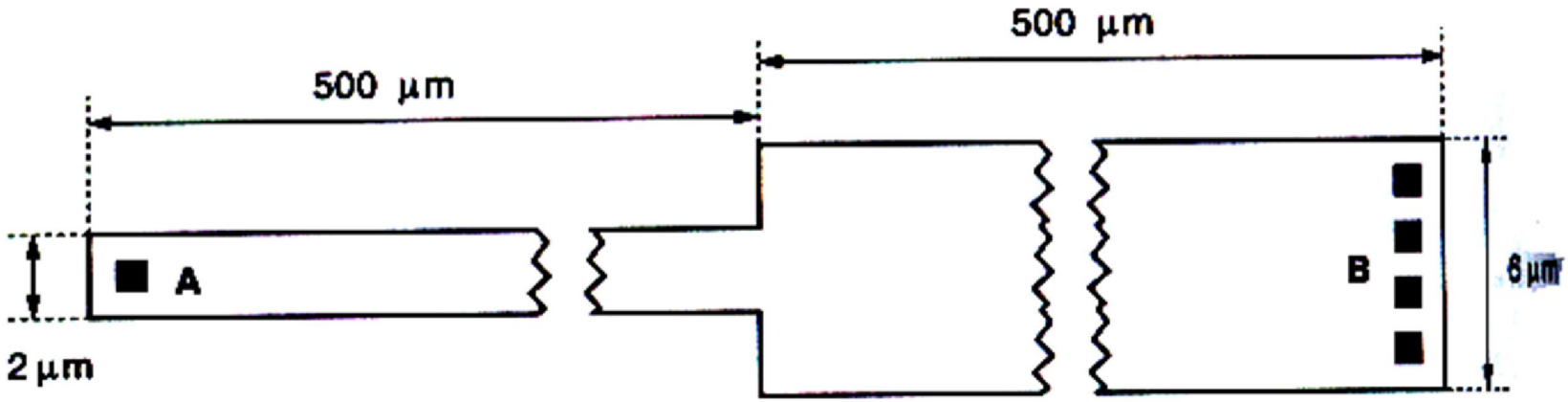
分布RC模型与集总RC模型的模拟结果



电路模拟中近似的分布RC模型

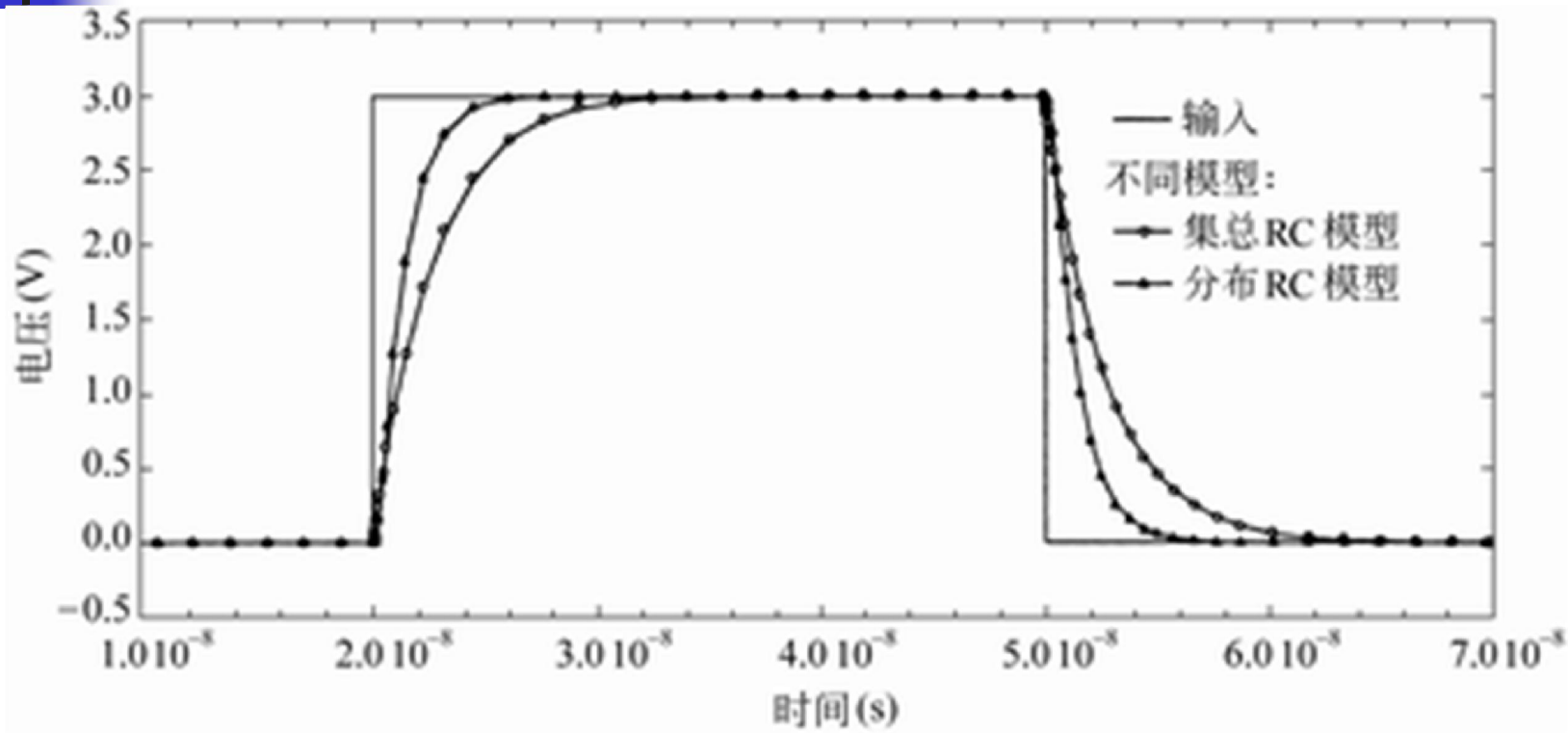


互连线RC延迟的模拟实例

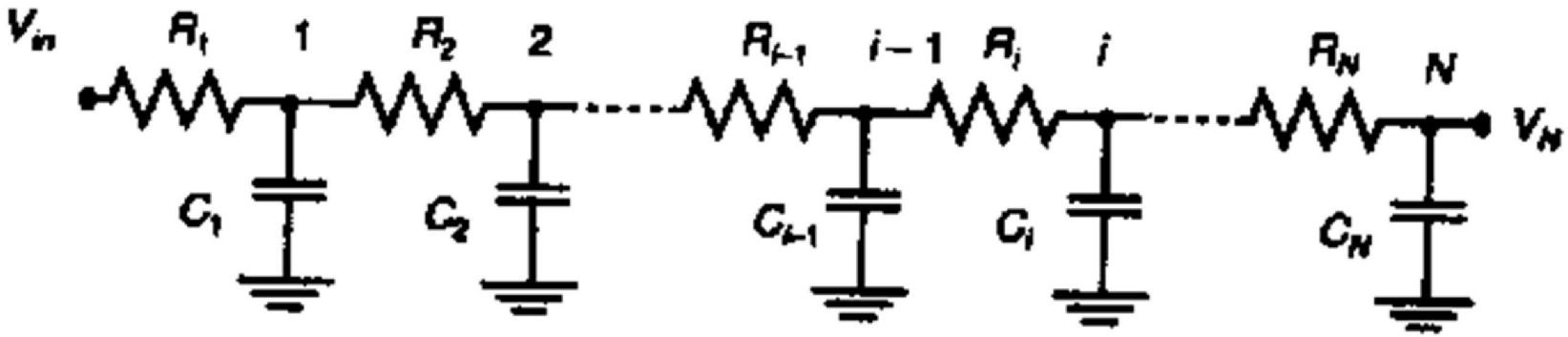


polysilicon interconnect line

互连线RC延迟的模拟结果



Elmore的RC网络延迟模型

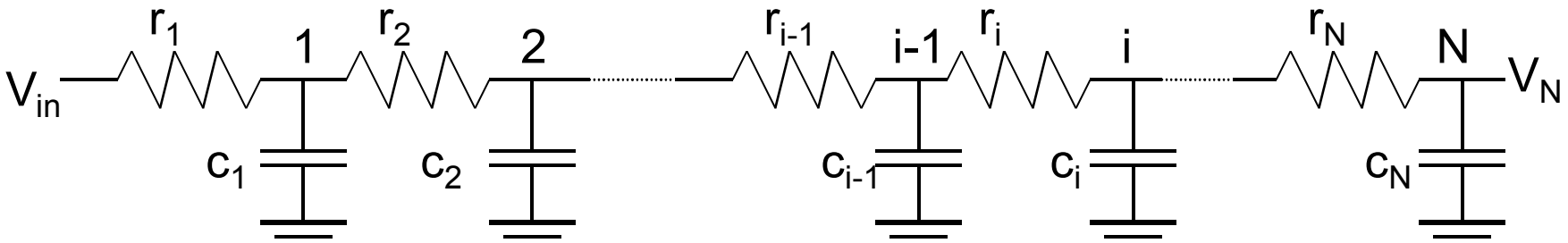


$$\tau = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

$$\tau_i = C_1 R_1 + C_2 (R_1 + R_2) + \cdots + C_i (R_1 + R_2 + \cdots + R_i)$$

Elmore模型

$\tau_{D1}=c_1r_1$ $\tau_{D2}=c_1r_1 + c_2(r_1+r_2)$

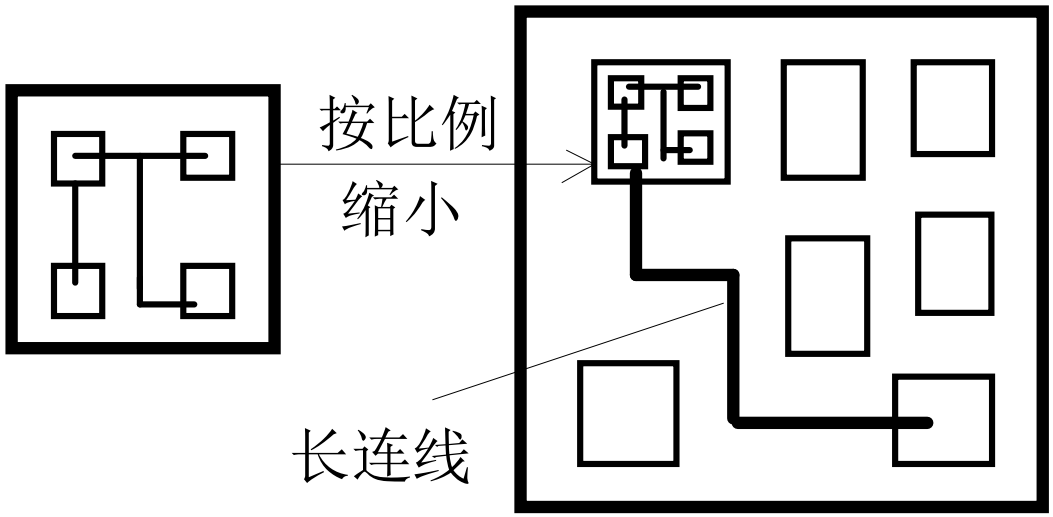


$\tau_{Di}=c_1r_1+ c_2(r_1+r_2)+\ldots+c_i(r_1+r_2+\ldots+r_i)$

Elmore delay equation $\tau_{DN} = \sum c_i r_{ii} = \sum^{N} c_i \sum^{i} r_j$

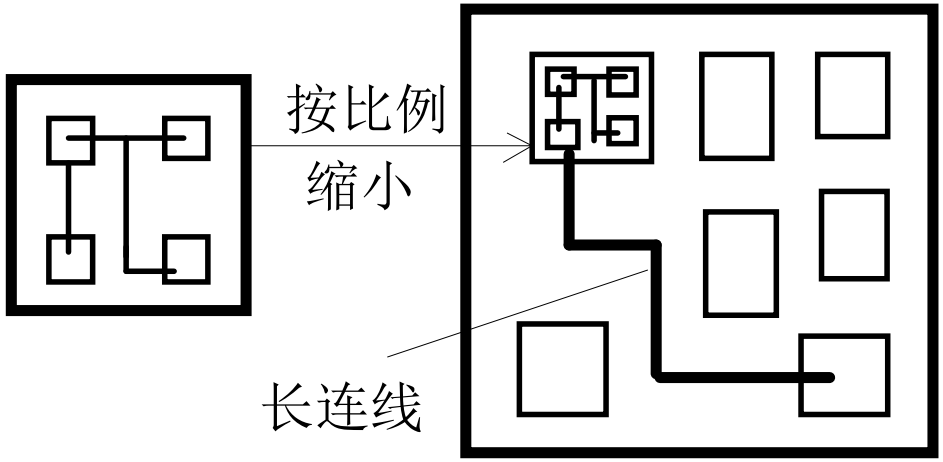
$\tau_{Di}=c_1r_{eq}+ 2c_2r_{eq}+ 3c_3r_{eq}+\ldots+ ic_ir_{eq}$

芯片面积增大引起的连线变化



$$L_m = \frac{\sqrt{A}}{2}$$

芯片面积增大引起的连线变化

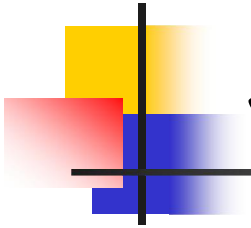


$$L_{\mathrm{M}} \approx \frac{\sqrt{A_{\mathrm{D}}}}{2}$$

$$t_{\mathrm{p}} = 0.69RC$$

$$= 0.69\rho \frac{L_{\mathrm{M}}}{W \cdot T} \cdot k\left(\frac{\varepsilon_0 \varepsilon_{\mathrm{ox}}}{H} W L_{\mathrm{M}} + \frac{\varepsilon_0 \varepsilon_{\mathrm{ox}}}{S} T L_{\mathrm{M}}\right)$$

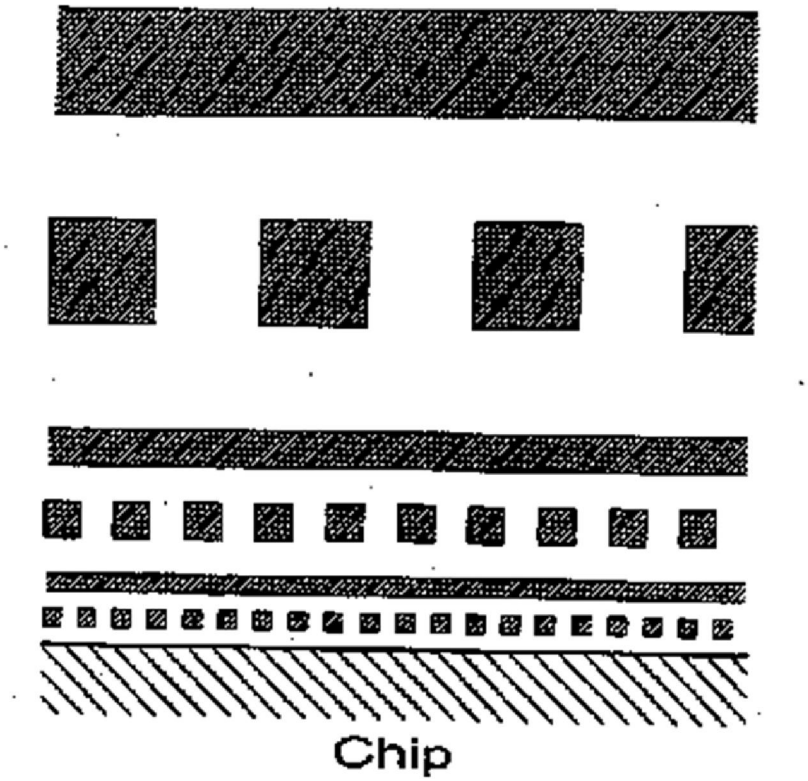
$$t_{\mathrm{p}} = \alpha \varepsilon_0 \varepsilon_{\mathrm{ox}} \rho \frac{A_{\mathrm{D}}}{\lambda^2}$$



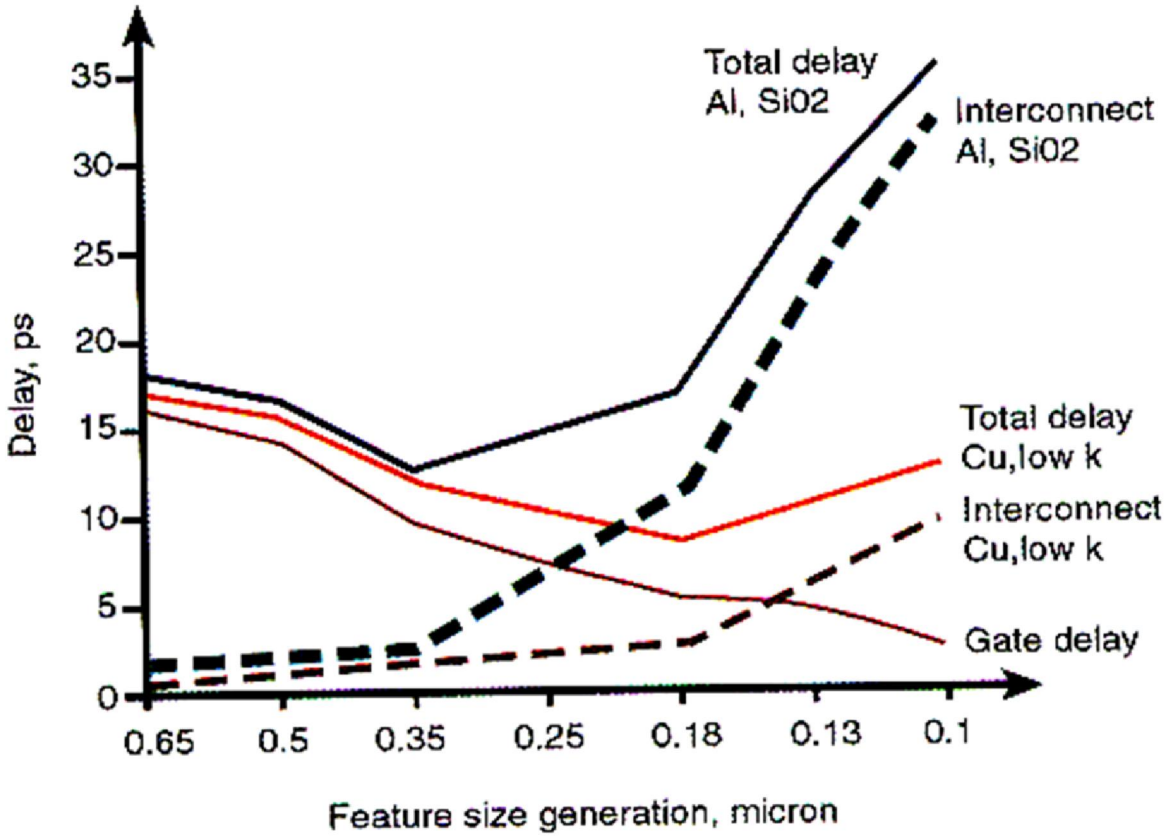
减小连线RC延迟的措施

- 合理的连线设计
- 优化的按比例缩小
- 多层互连技术
- 采用新的低阻连线材料
- 采用新的低*k*介质材料

多层互连技术



铜互连和低k介质



连线延迟的最终限制