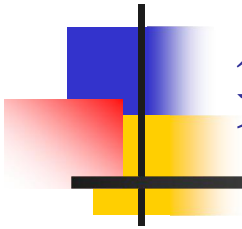
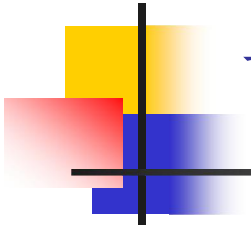


集成电路原理与设计

绪论及工艺原理



课程目标

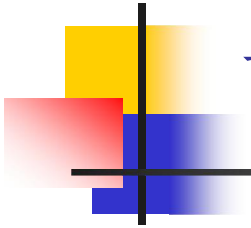
- 学习利用MOS器件构建数字集成电路
- 培养电路设计能力：根据不同设计要求（面积，速度，功耗和可靠性），进行电路分析和优化设计的能力

关于本课程

- 联系器件和电路知识：SOC、ULSI 、MEMS方向均需要
- 先修课程：工艺原理、器件物理、数字逻辑
- 后续课程：集成电路设计实习
- 考核方式：期末考试60%＋作业25%＋期中考试15%

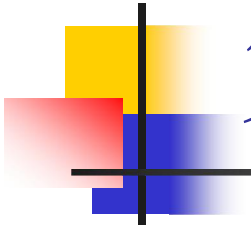
课程教材和参考书

- 教材：《集成电路原理与设计》
- 参考书：《数字集成电路－设计透视》，第二版，Rabaey等



课程信息

- 贾嵩：理科2号楼2703房间，62757449，13693165621，jias@pku.edu.cn
- 助教：刘俐敏（llmbird@126.com），洪杰（trevorwenwen520@163.com）
- 课程主页：北大教学网



第一章 绪论

- 集成电路的历史
- 集成电路的发展规律
- 等比例缩小原则
- 未来发展和挑战

集成电路的发展

- 第一个晶体管是那年发明的?

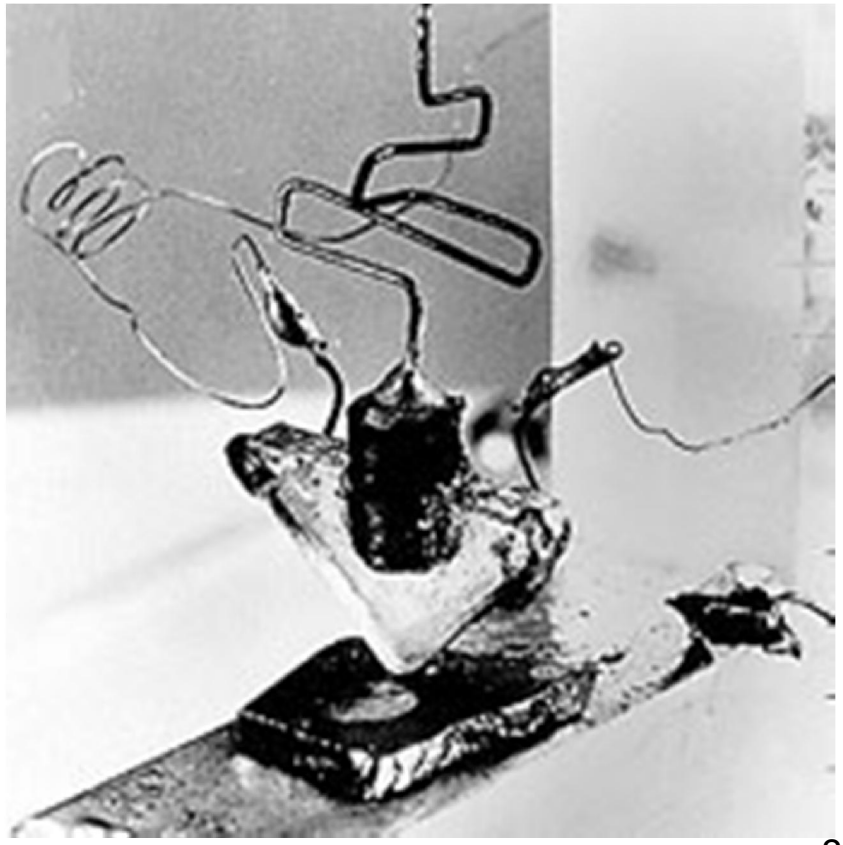
A. 1945 B. 1947 C. 1951 D. 1958

- 发明者当时供职与哪家公司?

A. IBM B. Bell Lab C. TI D. Motorola

第一个晶体管

- Modern-day electronics began with the invention in 1947 of the bi-polar transistor by Bardeen *et.al* at Bell Laboratories



The evolution of IC

- 第一块集成电路是那年做出来的?

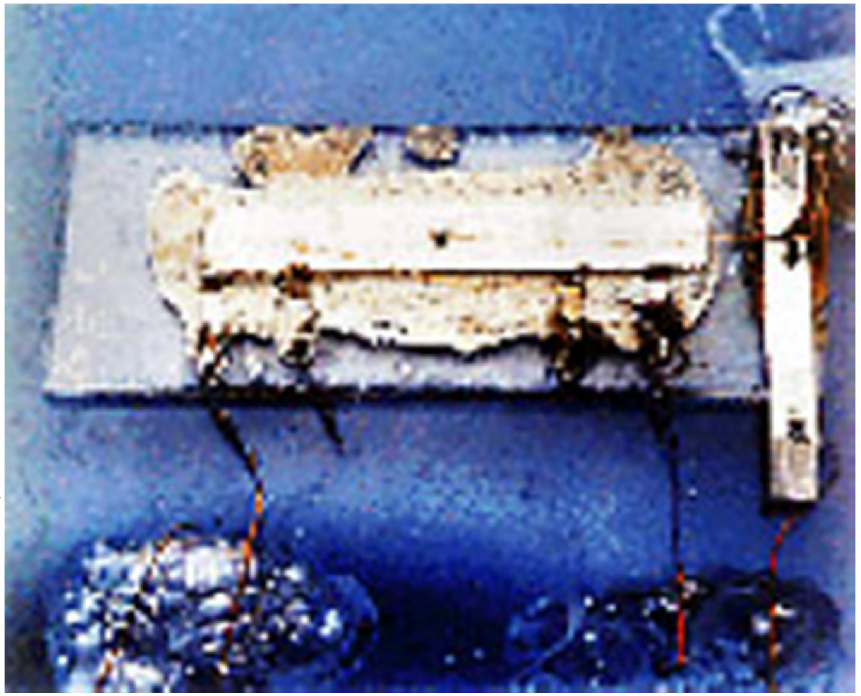
A. 1956 B. 1958 C. 1959 D. 1961

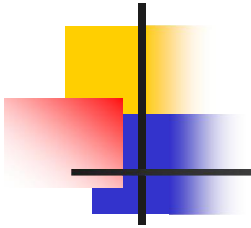
- 发明者当时供职于哪家公司?

A. IBM B. Bell Labs C. TI D. Motorola

第一块集成电路

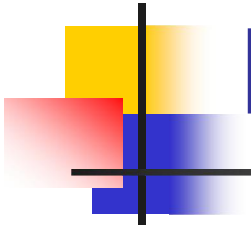
- In 1958 the integrated circuit was born when Jack Kilby at Texas Instruments successfully interconnected, by hand, several transistors, resistors and capacitors on a single substrate





晶体管发展

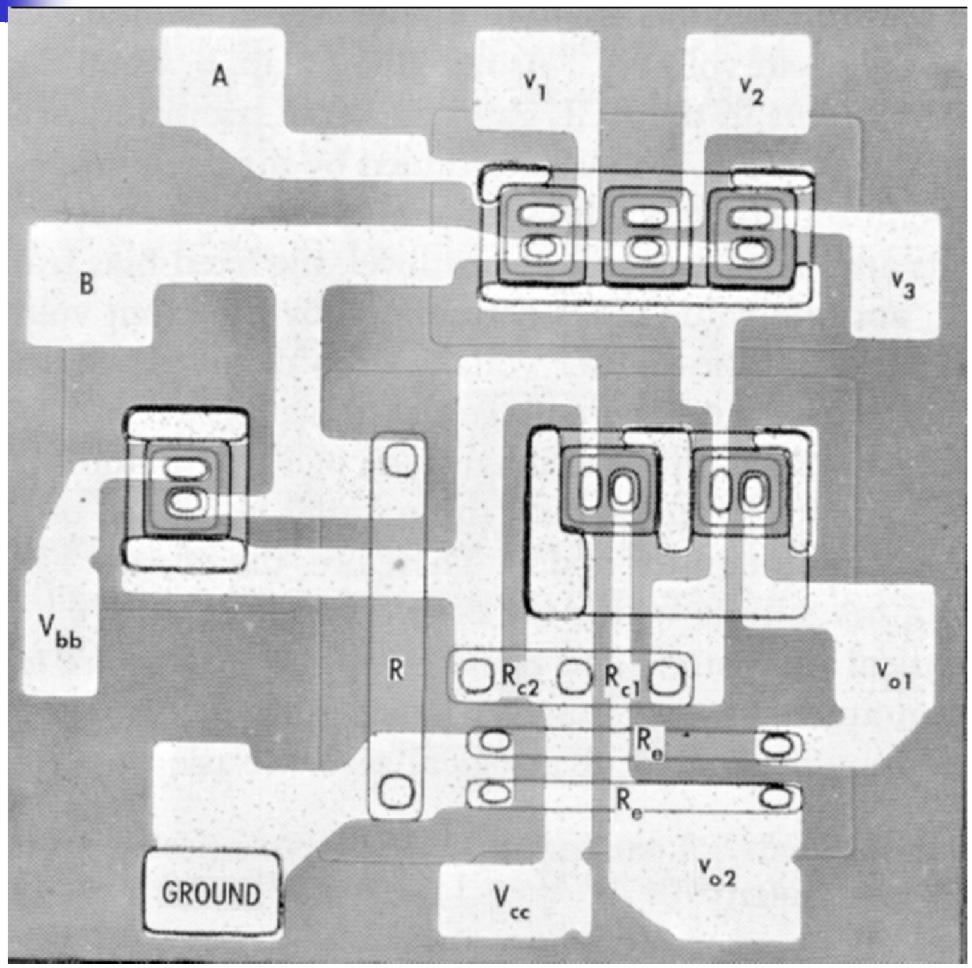
- Transistor –Bardeen *et.al.* (Bell Labs) in 1947
- Bipolar transistor – Schockley in 1948
- First monolithic IC – Jack Kilby in 1958
- First commercial IC logic gates – Fairchild 1960
- TTL – 1962 into the 1990's
- ECL – 1974 into the 1980's



MOSFET 工艺

- MOSFET transistor - Lilienfeld (Canada) in 1925 and Heil (England) in 1935
- CMOS – 1960's, 但是有很多工艺加工问题
- PMOS in 1960's (calculators)
- NMOS in 1970's (4004, 8080) – for speed
- CMOS in 1980's – 功耗优势
- BiCMOS, Gallium-Arsenide, Silicon-Germanium
- SOI, Copper-Low K, strained silicon, High-k gate oxide

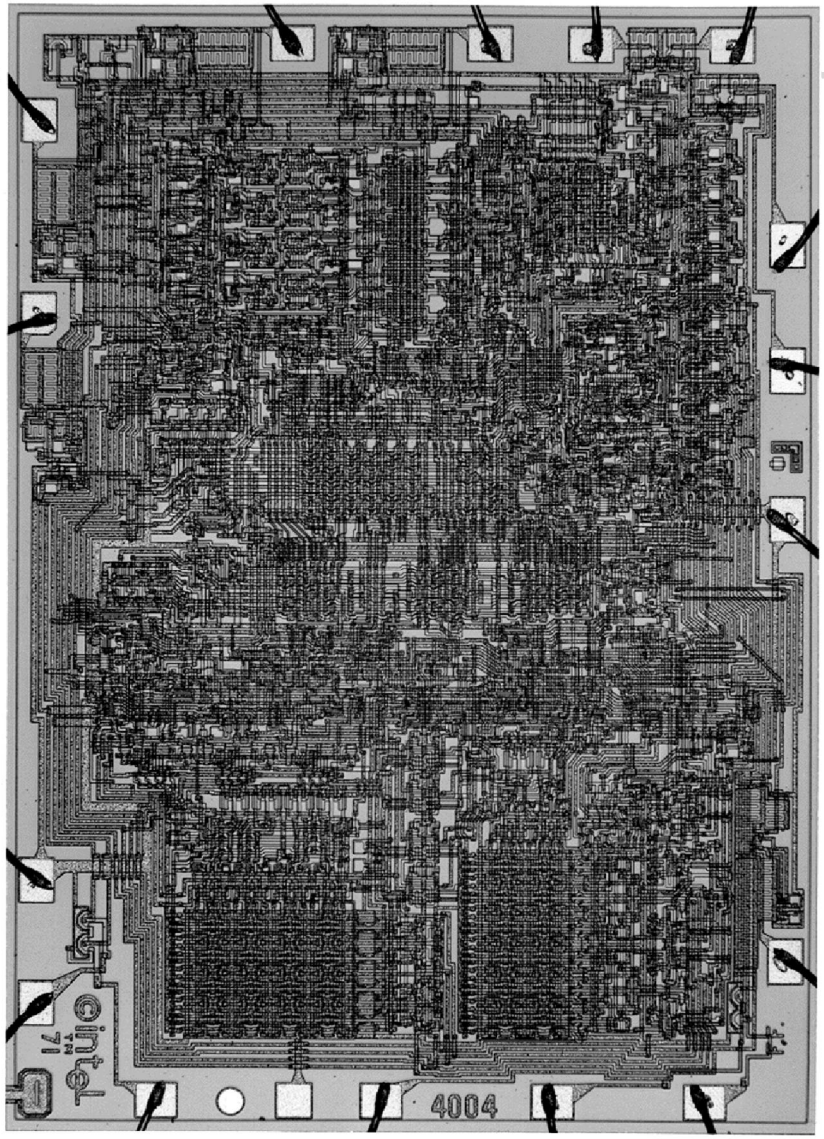
The First Integrated Circuits



Bipolar logic
1960's

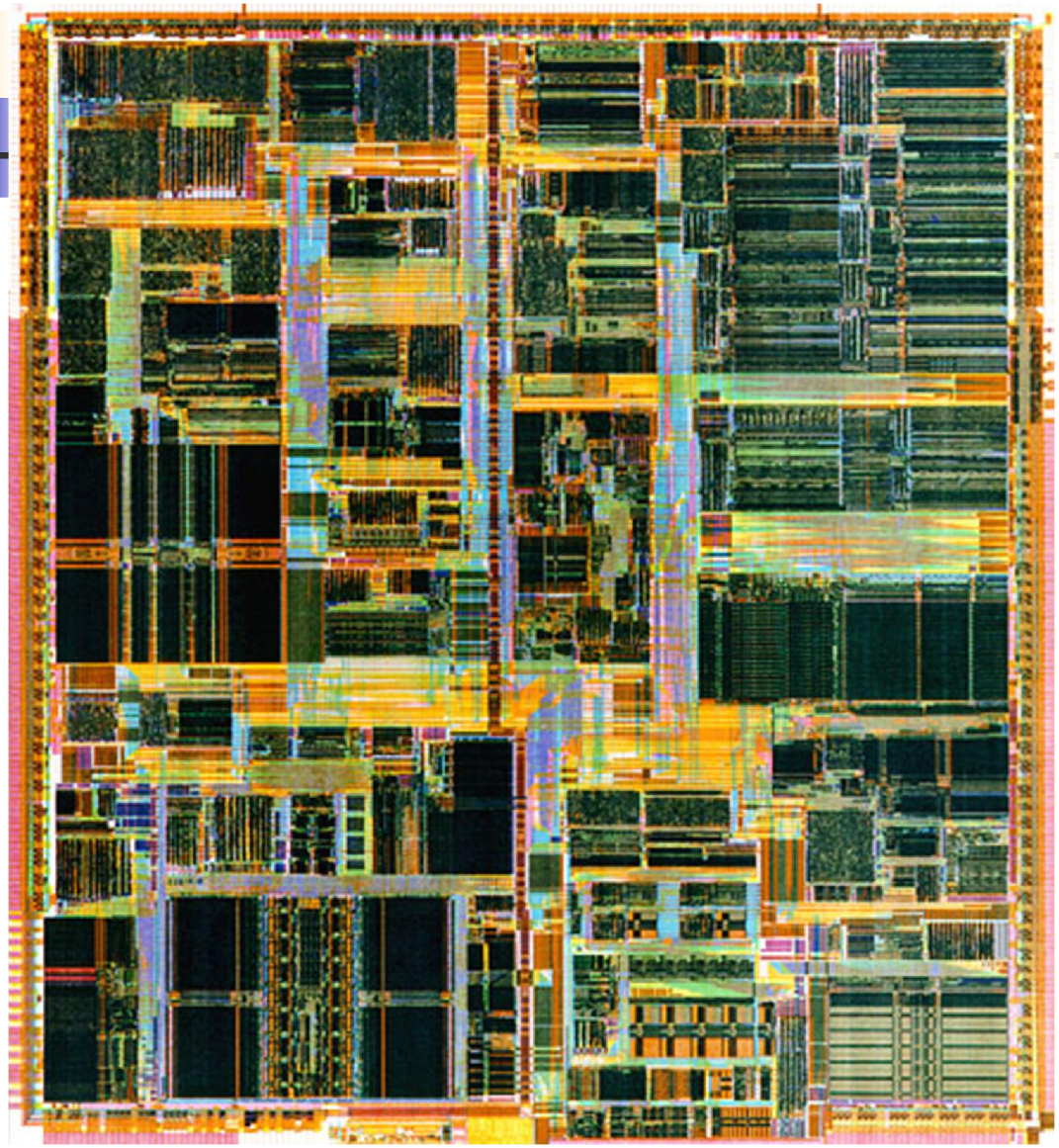
ECL 3-input Gate
Motorola 1966

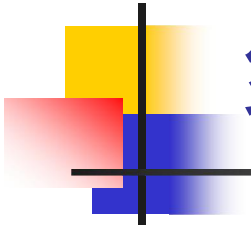
Intel 4004 Micro-Processor



1971
1000 transistors
1 MHz operation：
NMOS 工艺

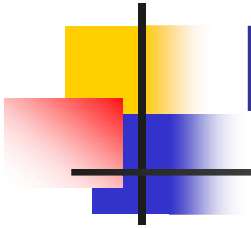
Intel Pentium (IV) microprocessor





绪论

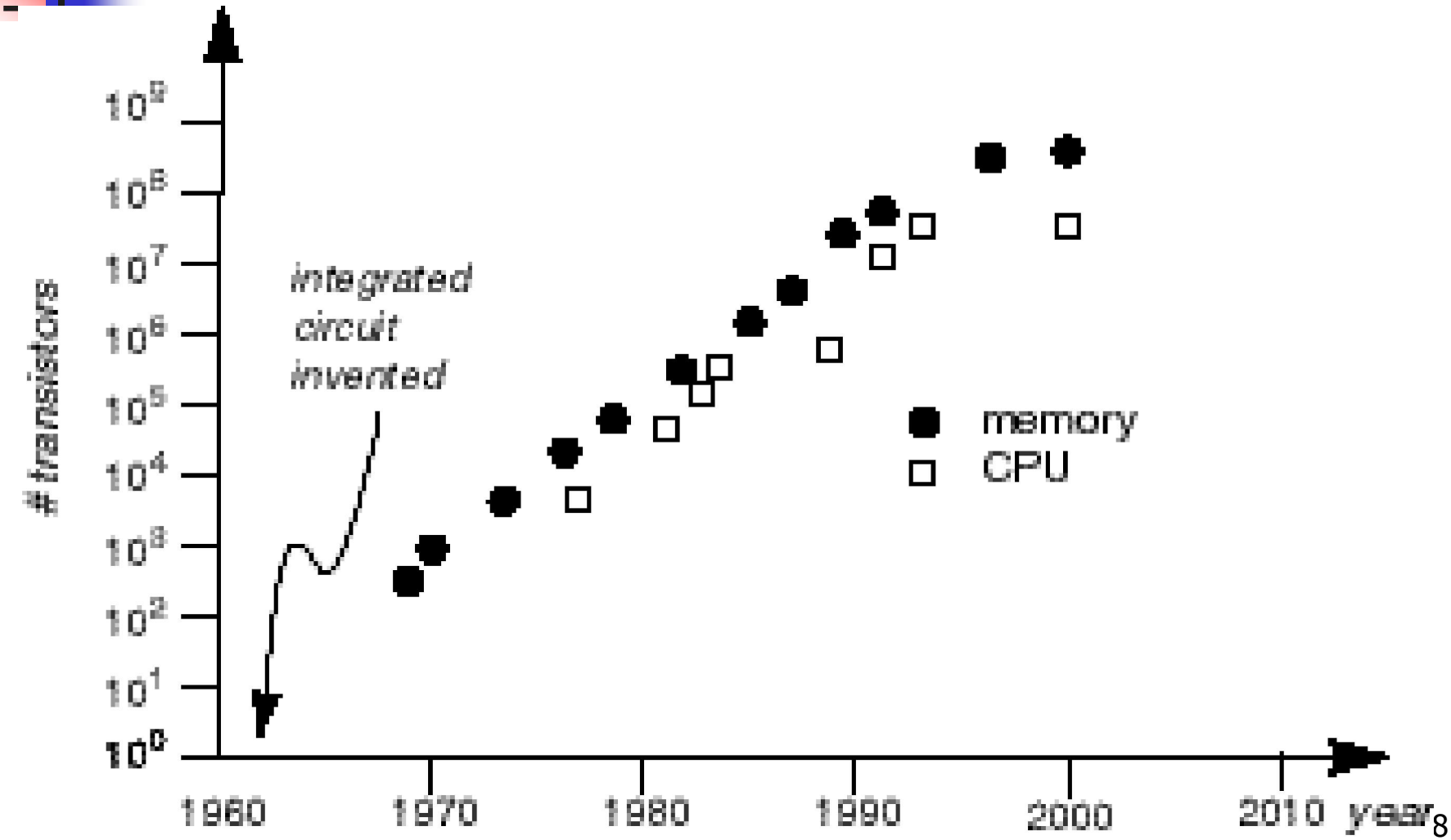
- 集成电路的历史
- 集成电路的发展规律
- 等比例缩小原则
- 未来发展和挑战



Moore's Law

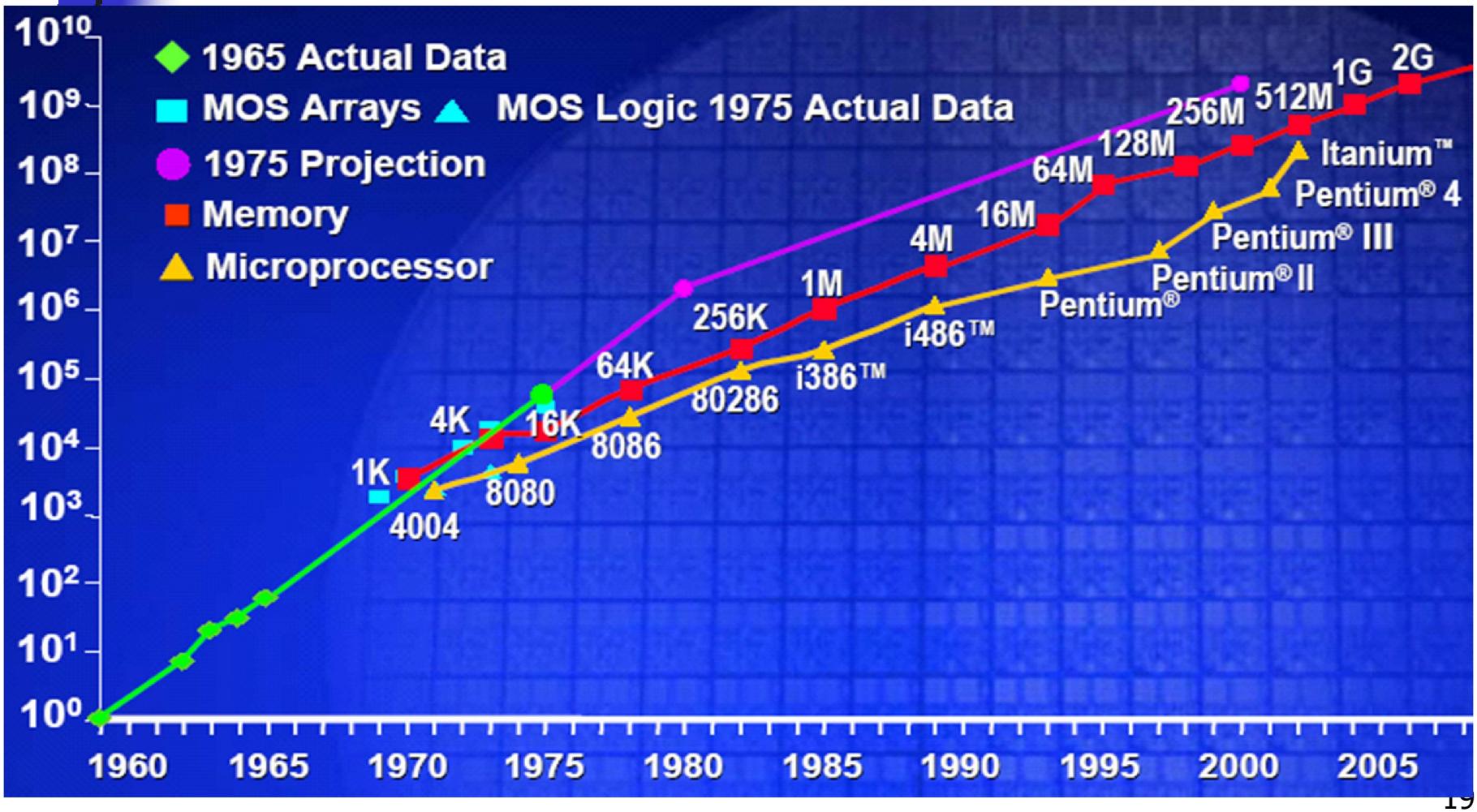
- 1965年，Gordon Moore预测单个芯片上集成的晶体管的数目每18个月可以增加一倍
  - 2300 transistors, 108 KHz clock (Intel 4004) - 1971
  - 16 Million transistors (Ultra Sparc III)- 1998
  - 42 Million, 2 GHz clock (Intel P4) - 2001
  - 125 Million, 3.4Ghz (Intel P4 Prescott)- 2004 Feb 02

Moore's Law plot (from his original paper)

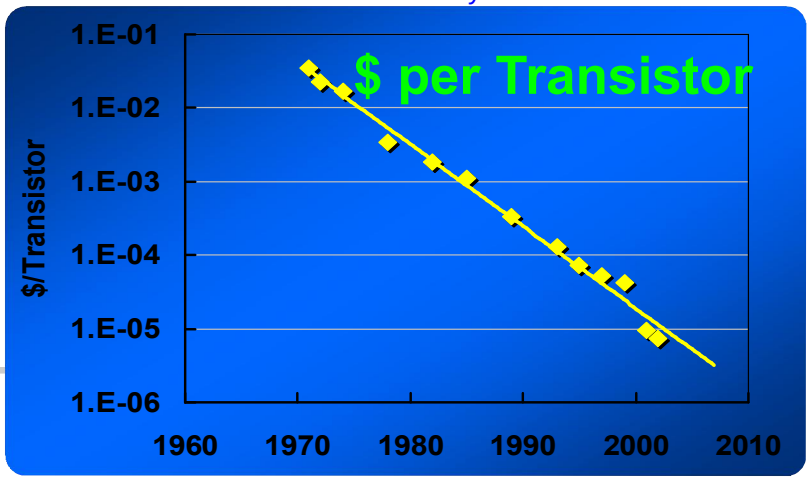


Source: ISSCC 2003 G. Moore "No exponential is forever, but 'forever' can be delayed"

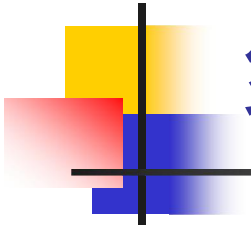
of Transistors per Die



摩尔定律——晶体管贬值



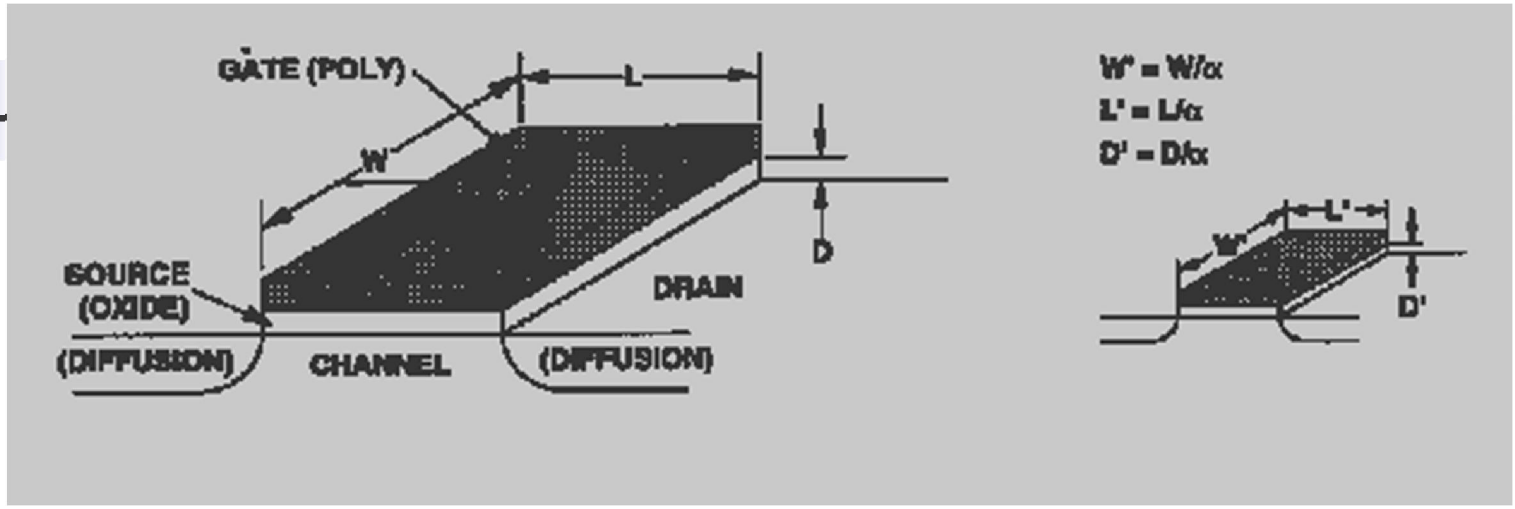
- Gordon Moore在1965年提出了摩尔定律，认为芯片上晶体管的数目每18个月增加1倍，这相当于每个晶体管的价格同步下降的过程
- 假设1965年一辆豪华跑车的售价是10万美元，如果该车的价格也能按照摩尔定律发展，则目前的售价如何？



绪论

- 集成电路的历史
- 集成电路的发展规律
- 等比例缩小原则
- 未来发展和挑战

MOS器件的发展：按比例缩小

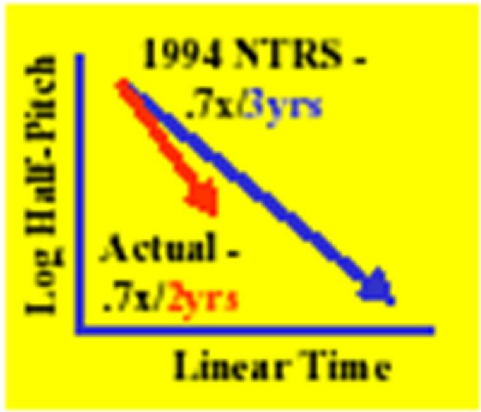


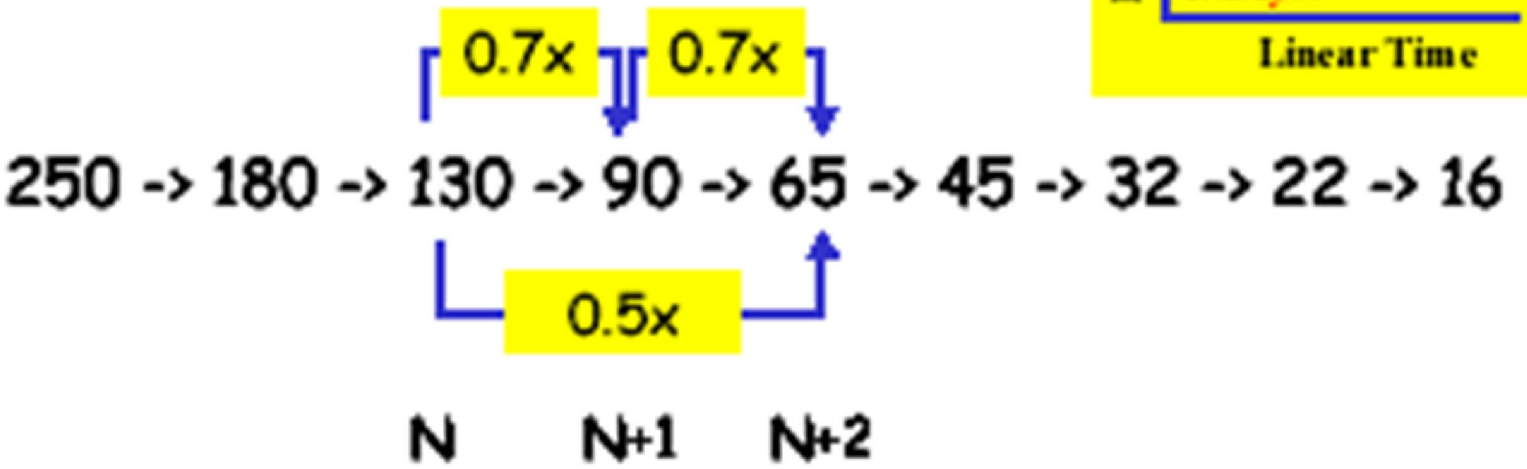
- 半导体工艺技术的发展遵循摩尔定律：
- 新工艺的特征尺寸是前代工艺的0.7倍，即器件密度为前代的2倍
- MOS器件的发展就是按比例缩小（scaling down）的过程

MOSFET缩小趋势

Scaling Calculator +

Node Cycle Time:

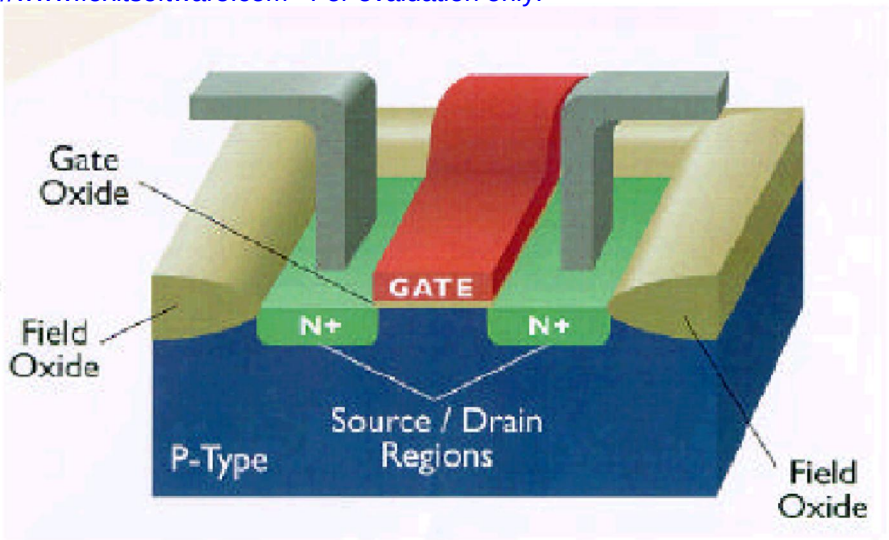




按比例缩小理论

- 为了跟上摩尔定律，器件尺寸不断缩小，短沟效应等二级效应出现，为了抑制二级效应，在器件按比例缩小过程中需要遵守一定的规则:
  - 恒定电场原则CE
  - 恒定电压原则CV
  - 准恒定电场原则QCE

按比例缩小：CE规则



- 器件的横向尺寸和纵向尺寸缩小 α 倍
- 外加电压按同样比例缩小
- 衬底掺杂浓度按同样比例增大
- 对于相邻两代工艺，　α ＝1.4

$$L' = L/\alpha,\ W' = W/\alpha,\ t_{ox}' = t_{ox}/\alpha,\ x_j' = x_j/\alpha$$

$$V_{DD}' = V_{DD}/\alpha$$

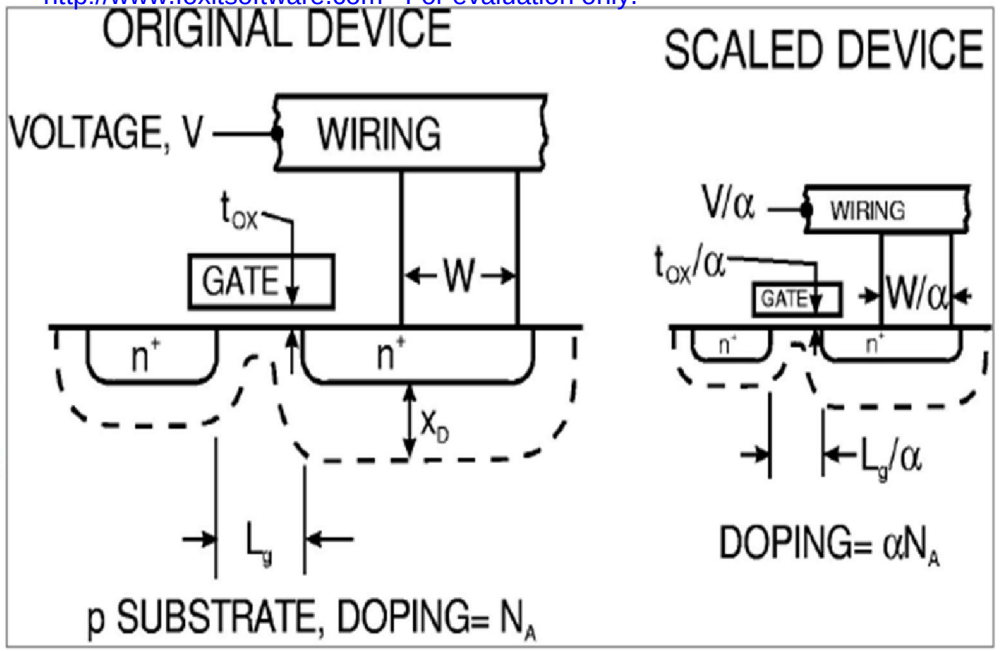
$$N_A' = \alpha N_A$$

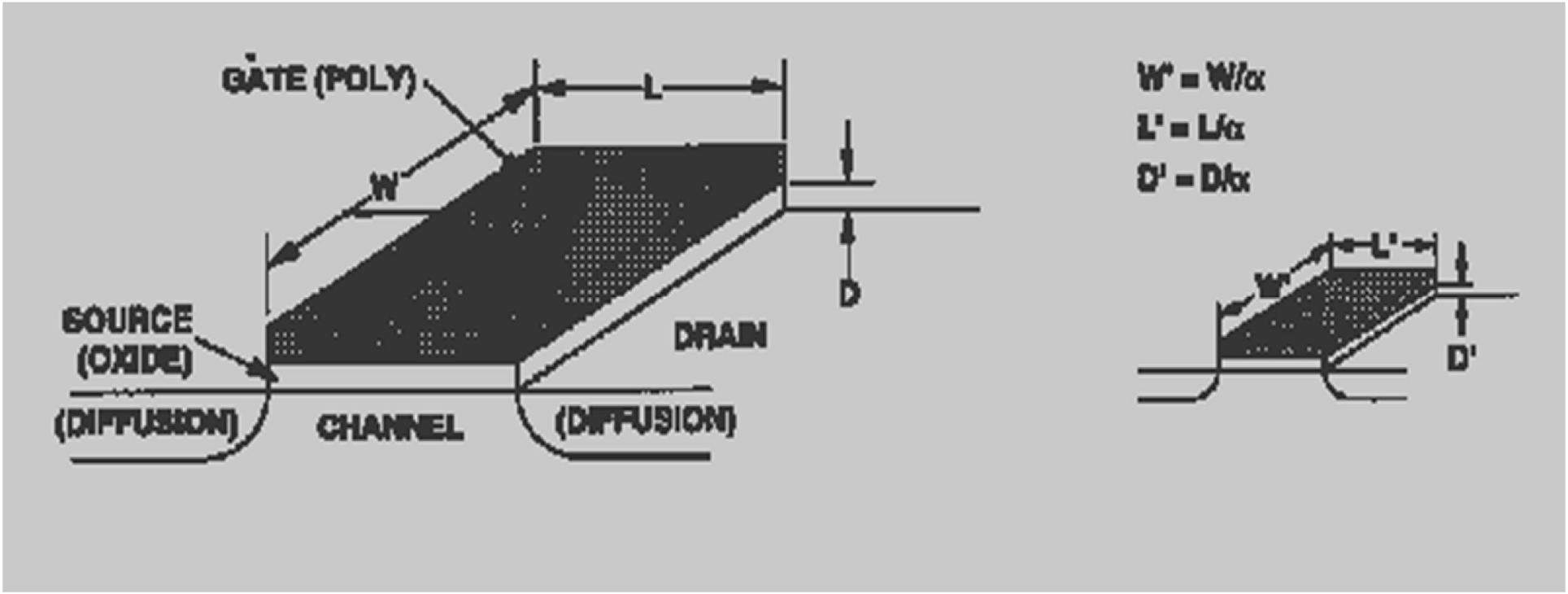
MOS器件按比例缩小

$$L' = L/\alpha,\ W' = W/\alpha,\ t_{ox}' = t_{ox}/\alpha,\ x_j' = x_j/\alpha$$

$$V_{DD}' = V_{DD}/\alpha$$

$$N_A' = \alpha N_A$$





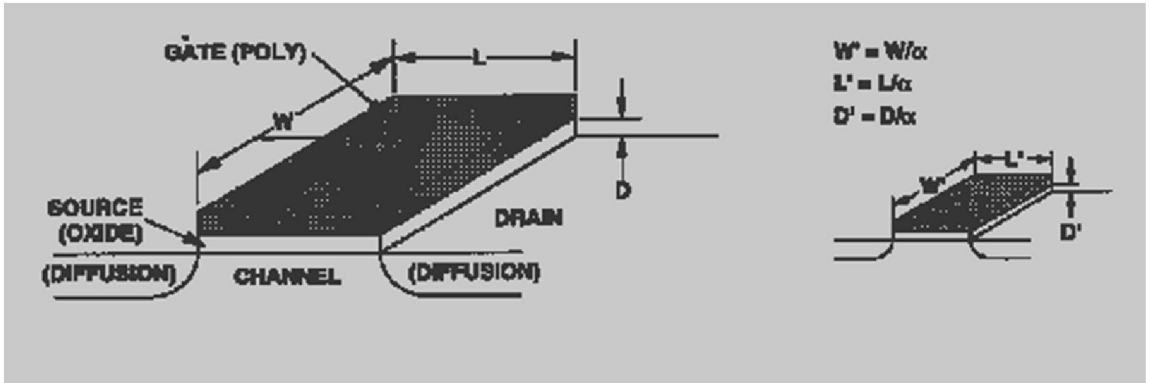
按CE规则缩小后的器件性能

1. 耗尽层厚度的变化

$$L' = L/\alpha,\ W' = W/\alpha,\ t_{ox}' = t_{ox}/\alpha,\ x_j' = x_j/\alpha$$

$$V_{DD}' = V_{DD}/\alpha$$

$$N_A' = \alpha N_A$$



➢CE中通过按比例降低工作电压和提高衬底掺杂浓度，可以使得源漏pn结耗尽区宽度实现按比例缩小

$$X_d = \left[\frac{2\varepsilon_0\varepsilon_{si}}{qN_A}\left(V_{bi} + V_{DS} - V_{BS}\right)\right]^{1/2}$$

$$X_d' = \left[\frac{2\varepsilon_0\varepsilon_{si}}{qN_A'}\left(V_{bi} + V_{DS}' - V_{BS}'\right)\right]^{1/2} \approx X_d/\alpha$$

2. 阈值电压的变化

➢阈值电压不是严格的按比例缩小

$$V_T' \approx -\frac{Q_{ox}}{C_{ox}'} + \frac{\sqrt{2\varepsilon_0\varepsilon_{si}qN'(2\varphi_F' - V_{BS}')}}{C_{ox}'}$$

$$\approx \frac{1}{\alpha}\left[-\frac{Q_{ox}}{C_{ox}} + \frac{1}{C_{ox}}\sqrt{2\varepsilon_0\varepsilon_{si}qN_A(2\varphi_F - V_{BS})}\right]$$

$$\approx V_T / \alpha$$

3. 工作电流的变化

- 按CE规则缩小的器件的导通电流按比例缩小

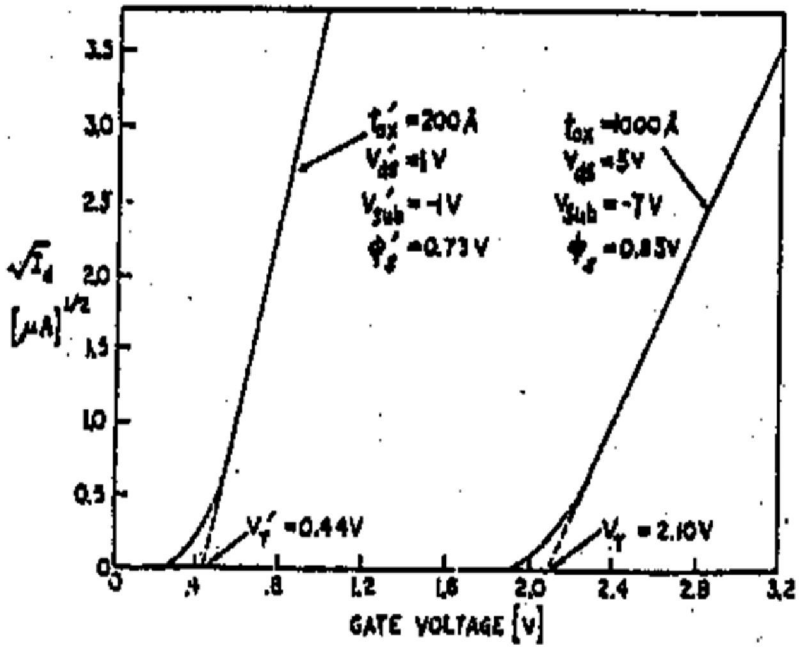
$$I'_D = \frac{W'}{L'}\mu_{\text{eff}}C'_{ox}\left[\left(V'_{GS}-V'_T\right)-\frac{1}{2}V'_{DS}\right]\cdot V'_{DS}$$

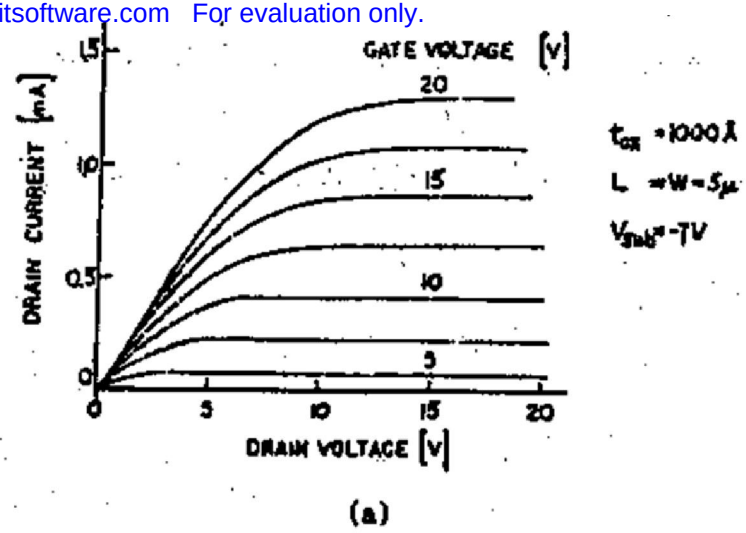
- 由于沟道宽度W按比例缩小，因此器件的沟道电流密度不变

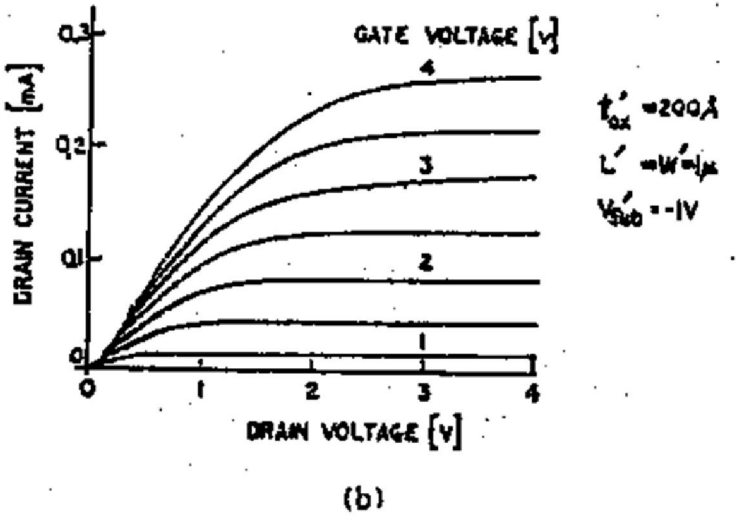
$$I'_D = I_D / \alpha$$

- 器件的导电因子增加 α 倍

MOS器件缩小前后的输入和输出特性







- 根据实际测量的结果，按比例缩小后的器件基本符合CE规则的预计

4.延迟时间和功耗的变化

$$t'_d = \frac{C'_L \cdot V'}{I'_D} = t_d / \alpha \qquad P_D{}' = f' C_L' (V'_{DD})^2 = \alpha f \frac{C_L}{\alpha}\left(\frac{V_{DD}}{\alpha}\right)^2 = P_D \Big/ \alpha^2$$

- 按比例缩小后，器件的特性基本按比例变化
- 性能：速度按比例增加
- 功耗：由于电流和电压按比例缩小，功耗按照平方的关系缩小

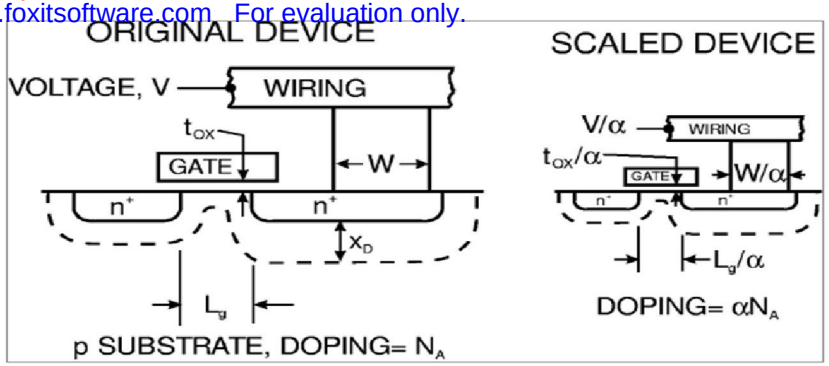
按比例CE规则对电路影响

$$(PDP)' = P't'_d = PDP / \alpha^3$$

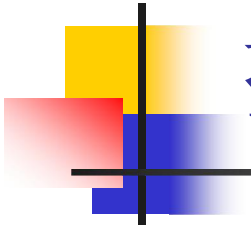
- 综合考虑速度和功耗的参数PDP按3次方减小，而面积，按照平方减小
- 可见，CE规则变化的器件集成度按平方增加，速度线性增加，而功耗平方减小
- 这就是为什么人们不断追求半导体工艺的进步的主要原因

按比例变化CE

α >1



工艺参数的按比例缩小	器件尺寸（Tox，L，W，Xj）	1/ α
	掺杂浓度（Na，Nd）	α
	电源电压（Vdd）	1/ α
器件参数的变化	电场	1
	载流子速度	1
	耗尽区宽度	1/ α
	电容	1/ α
	漂移电流	1/ α
	沟道电阻	1
电路参数的变化	电路的延迟(T~CV/I)	1/ α 好
	器件的功耗(P~VI)	$1/\alpha^2$ 很好
	功耗延迟乘积PDP(=PT)	$1/\alpha^3$ 非常好



按比例缩小理论

- 恒定电场原则CE
- 恒定电压原则CV
- 准恒定电场原则QCE

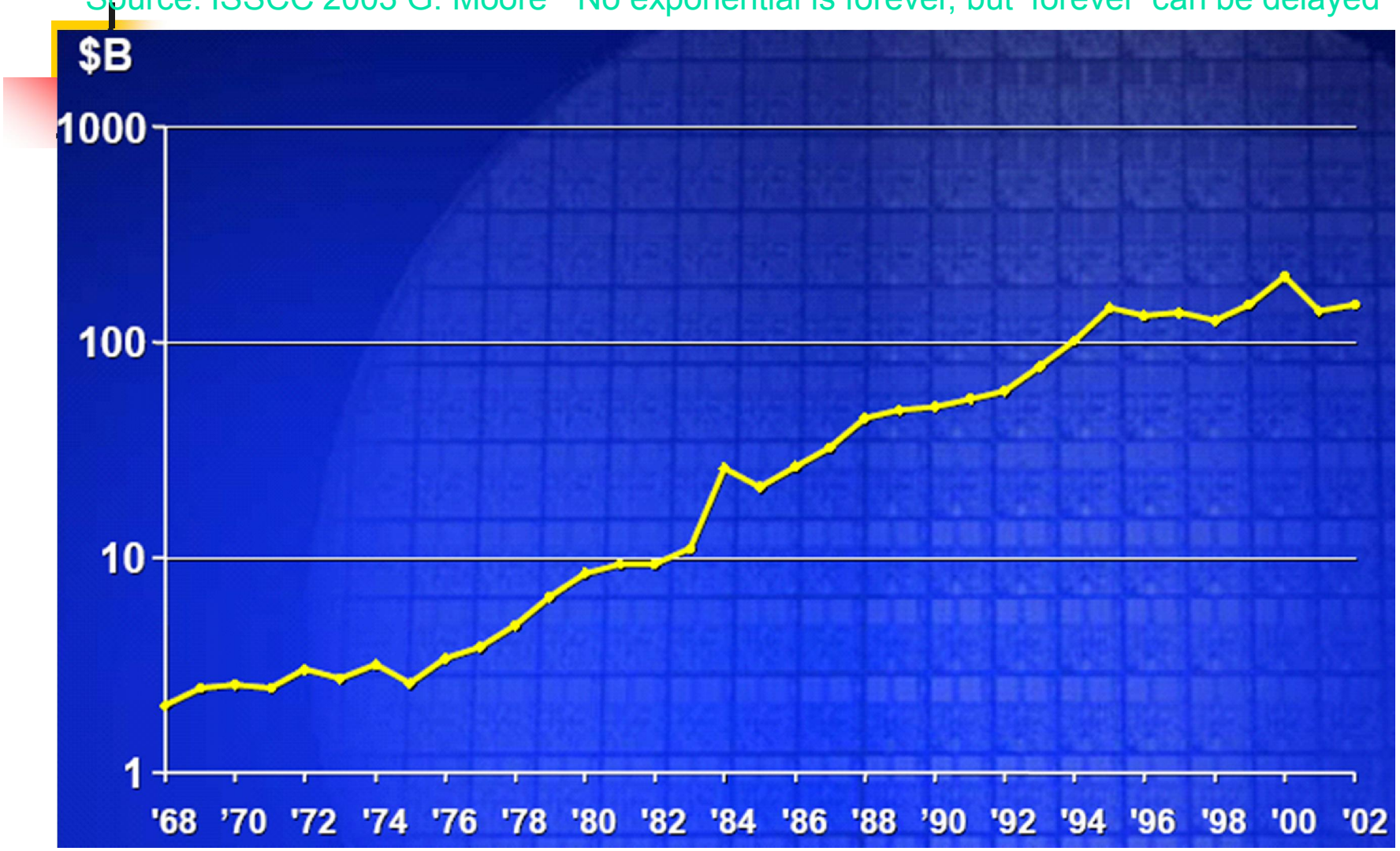
Silicon's Roadmap

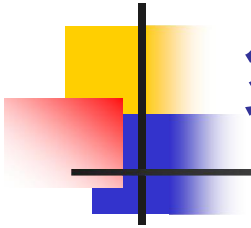
Year	1999	2002	2005	2008	2011	2014
Feature size (nm)	180	130	100	70	50	35
Chip size (mm^2)	170	214	235	269	308	354
Clock rate (GHz)*	1.2	1.6	2.2	2.8	3.6	4.4
Power supply V_{dd} (V)	1.8	1.5	1.2	0.9	0.7	0.6
Power (W)	90	130	160	170	174	183

For a Cost-Performance MPU
(L1 on-chip SRAM cache; 32KB in 1999 doubling every two years)

Worldwide Semiconductor Revenue

Source: ISSCC 2003 G. Moore "No exponential is forever, but 'forever' can be delayed"





绪论

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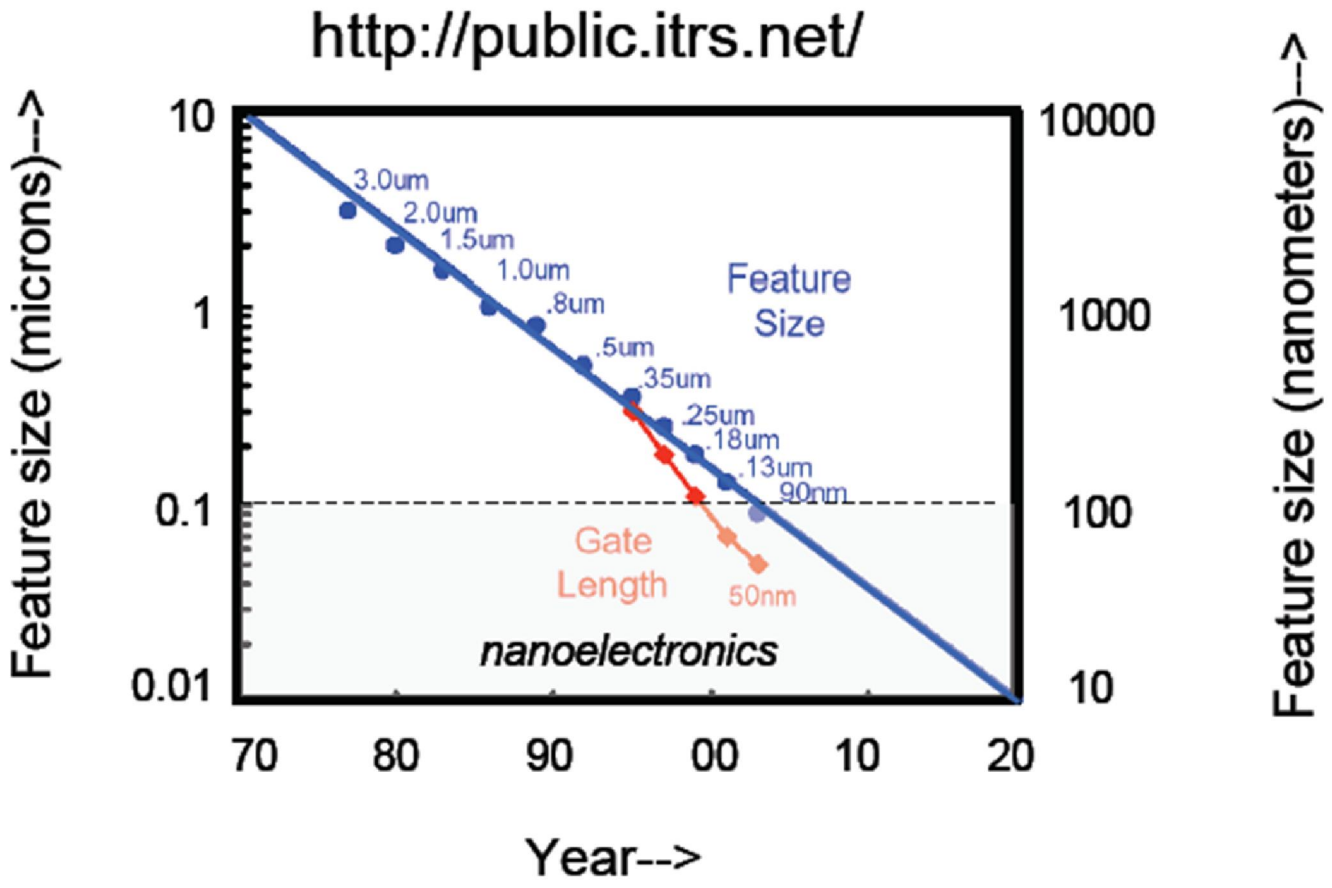
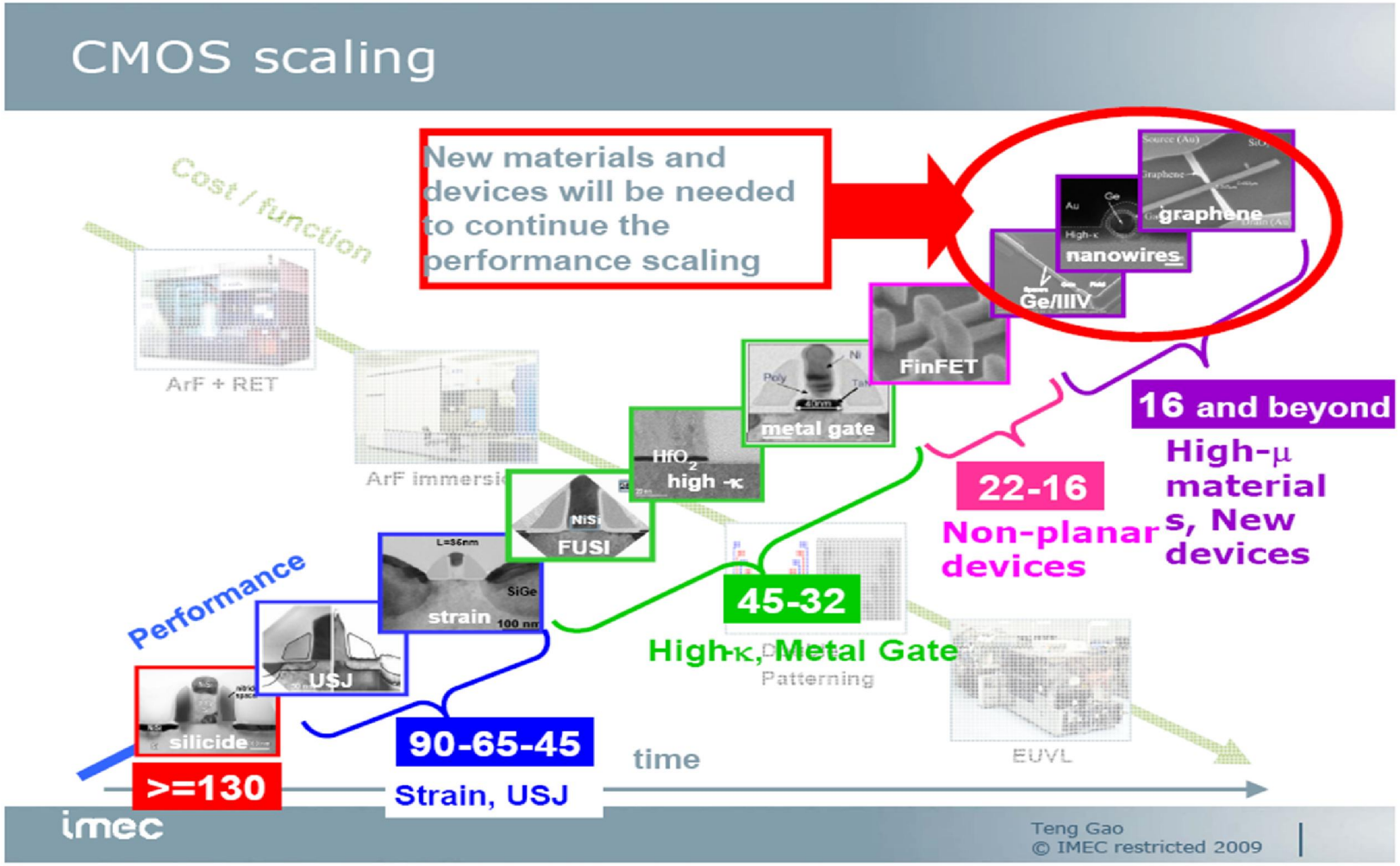
Gate Length Scaling



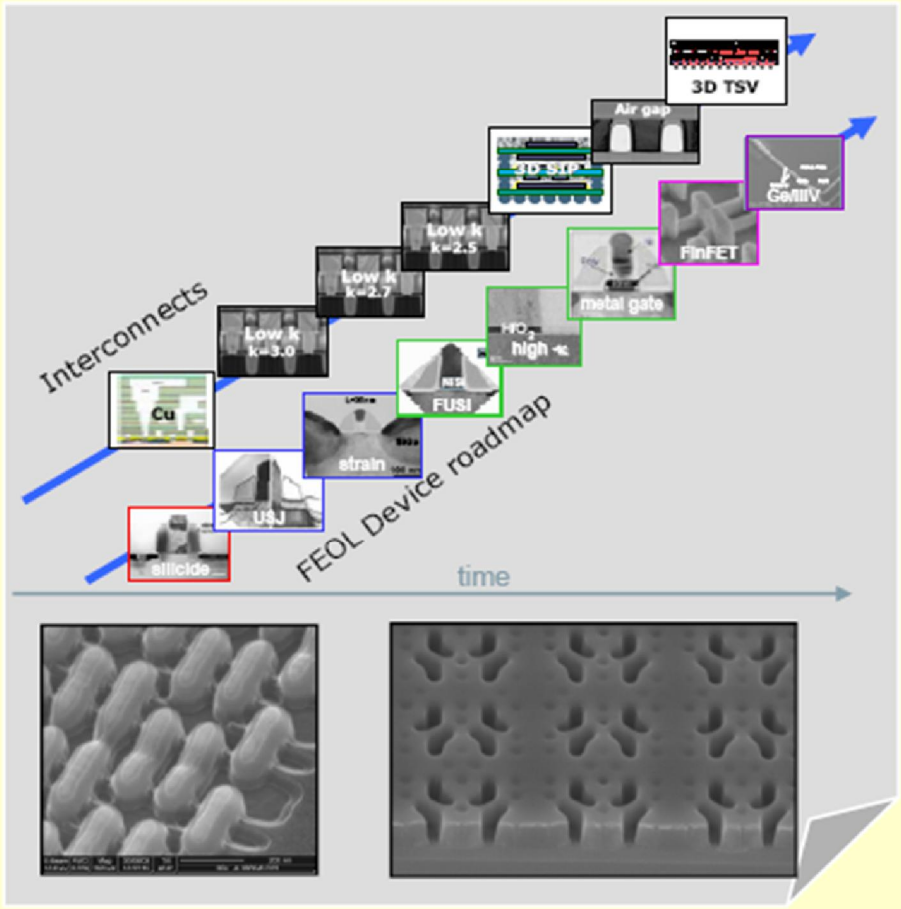
(L = 6 nm (IBM, 2002)
L = 5 nm (NEC, 2003))

微电子未来发展—more moore

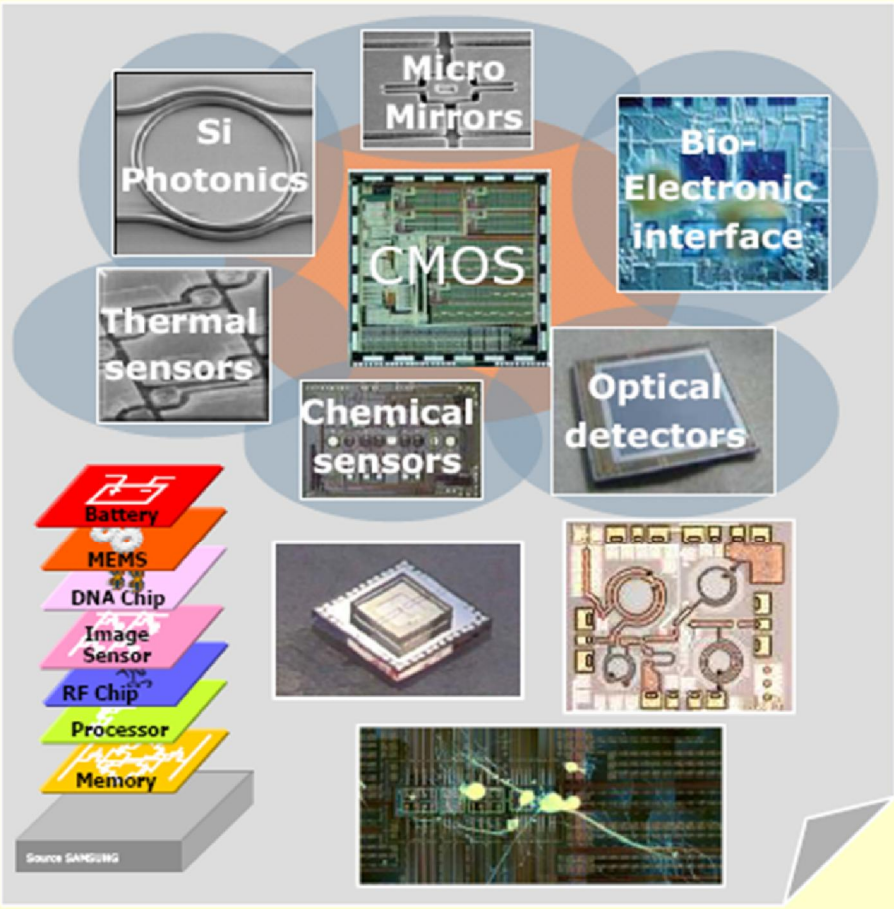


微电子未来发展—more than moore

More Moore



More than Moore



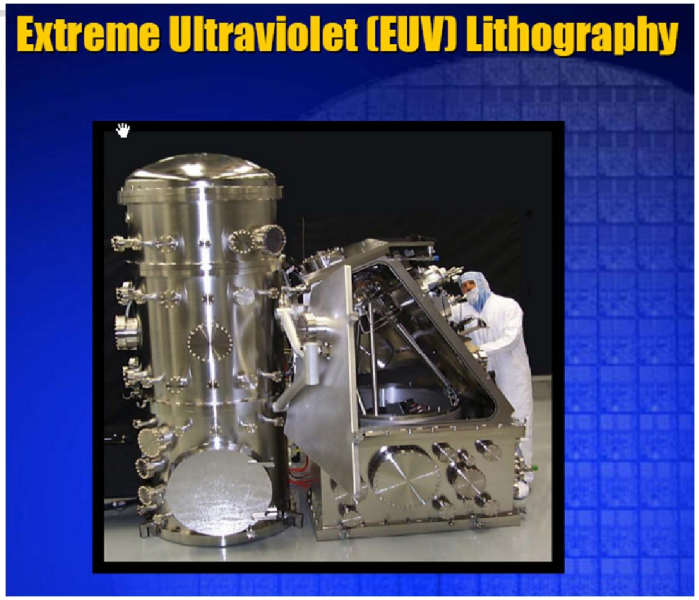
微电子未来挑战：物理极限

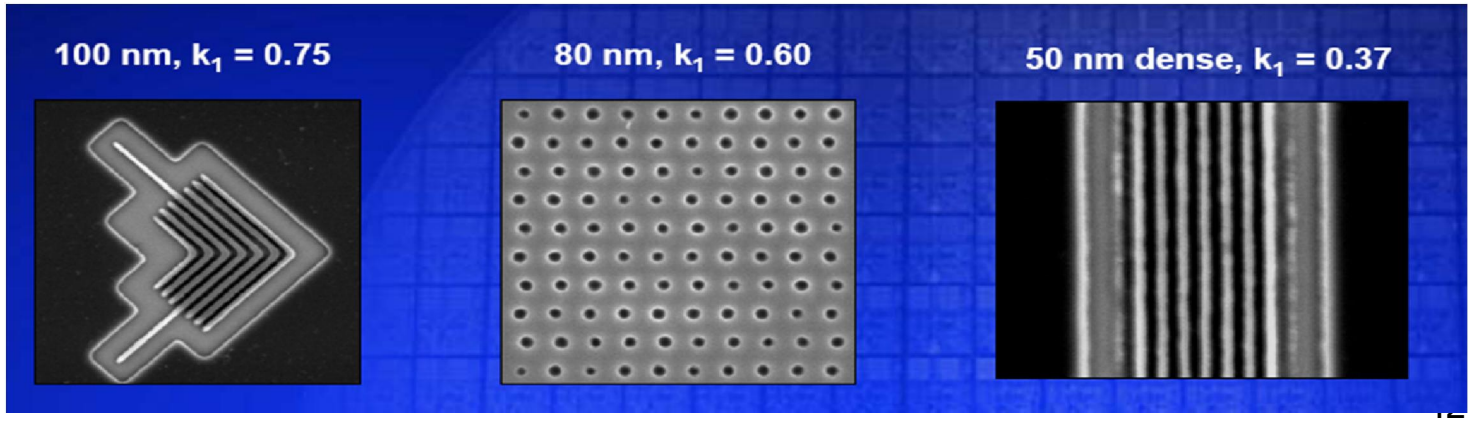
- 1999 – 1000 electrons to change state
- 2010 – 8 electrons to change state
- 2020 - < 1 electron to change state

Source: California Computer News, 2003

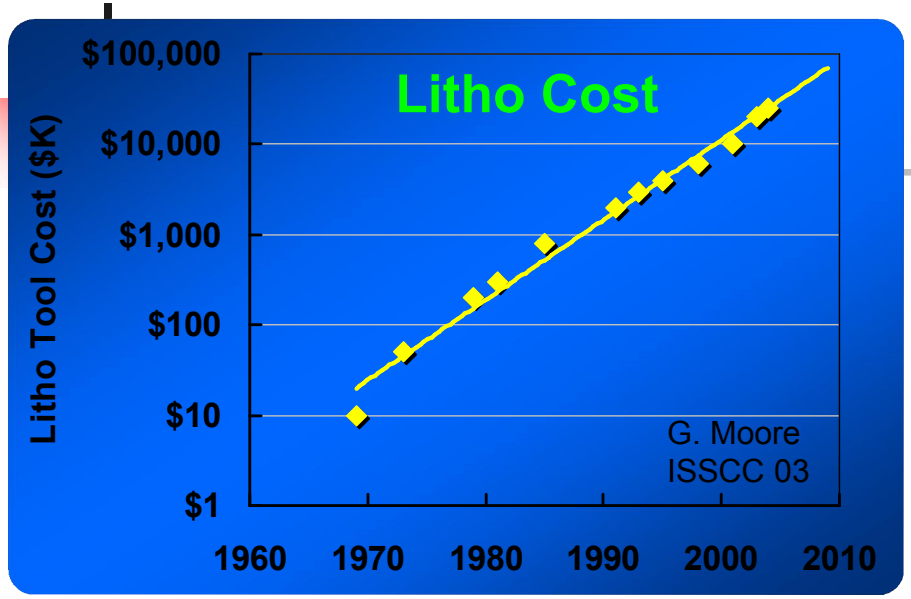
微电子未来挑战：工艺技术

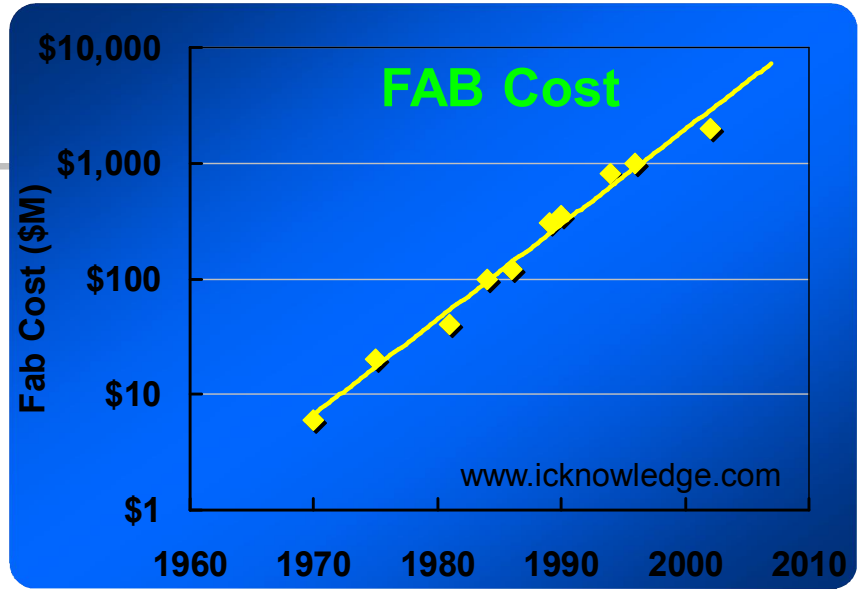
- 光刻线条
- 晶圆尺寸

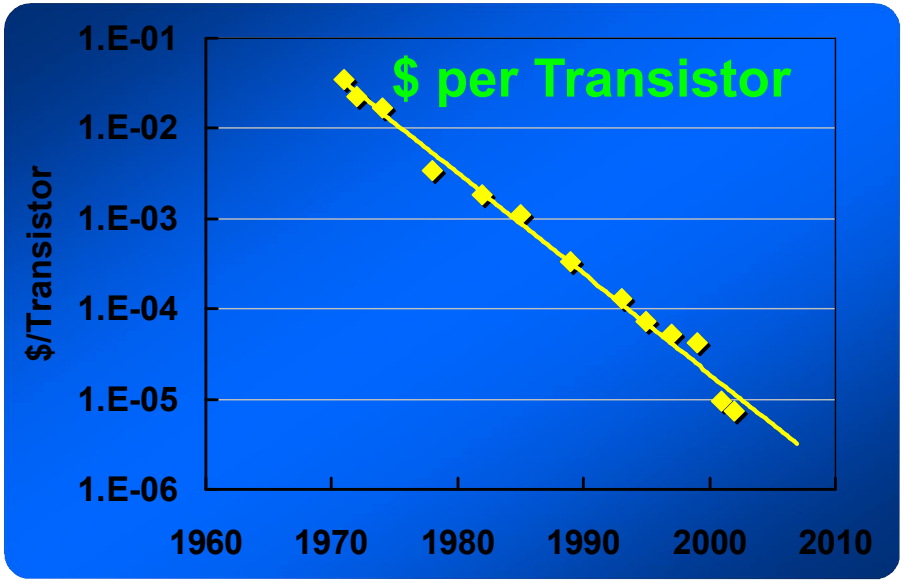


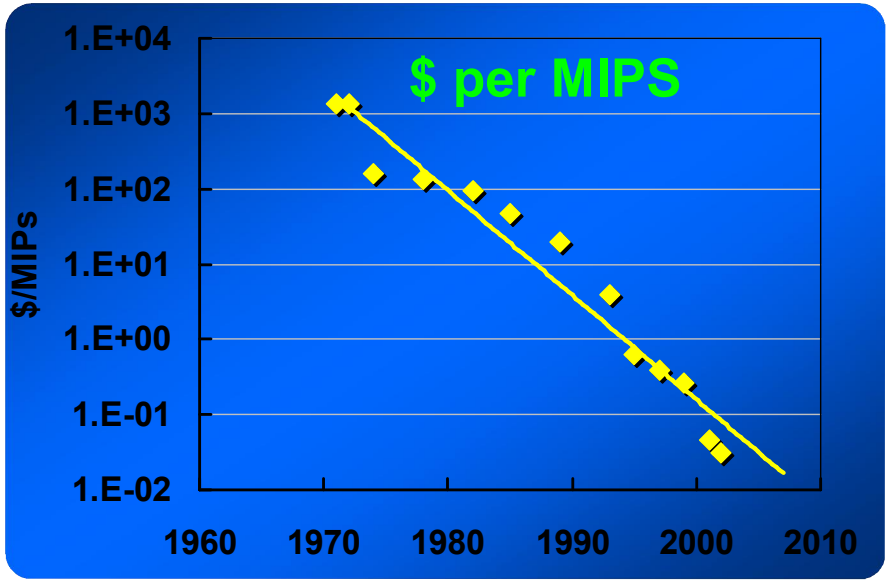


微电子未来挑战：经济因素



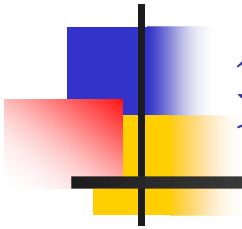






经济因素：加工费用

- 研制成本每代产品增加1.5倍
- 增加工艺步骤每代成本增加1.3倍
- 设备费用
- 封装价格
- 能源价格



集成电路原理与设计

集成电路制作工艺：工艺基础

第二章 集成电路制作工艺

- 2.1.1 集成电路加工的基本操作
- 2.1.2 MOS结构和分类
- 2.2.1 N阱CMOS工艺
- 2.2.2 深亚微米CMOS工艺
- 2.3.1 CMOS IC中的寄生效应
- 2.3.2 SOI工艺
- 2.3.3 CMOS版图设计规则

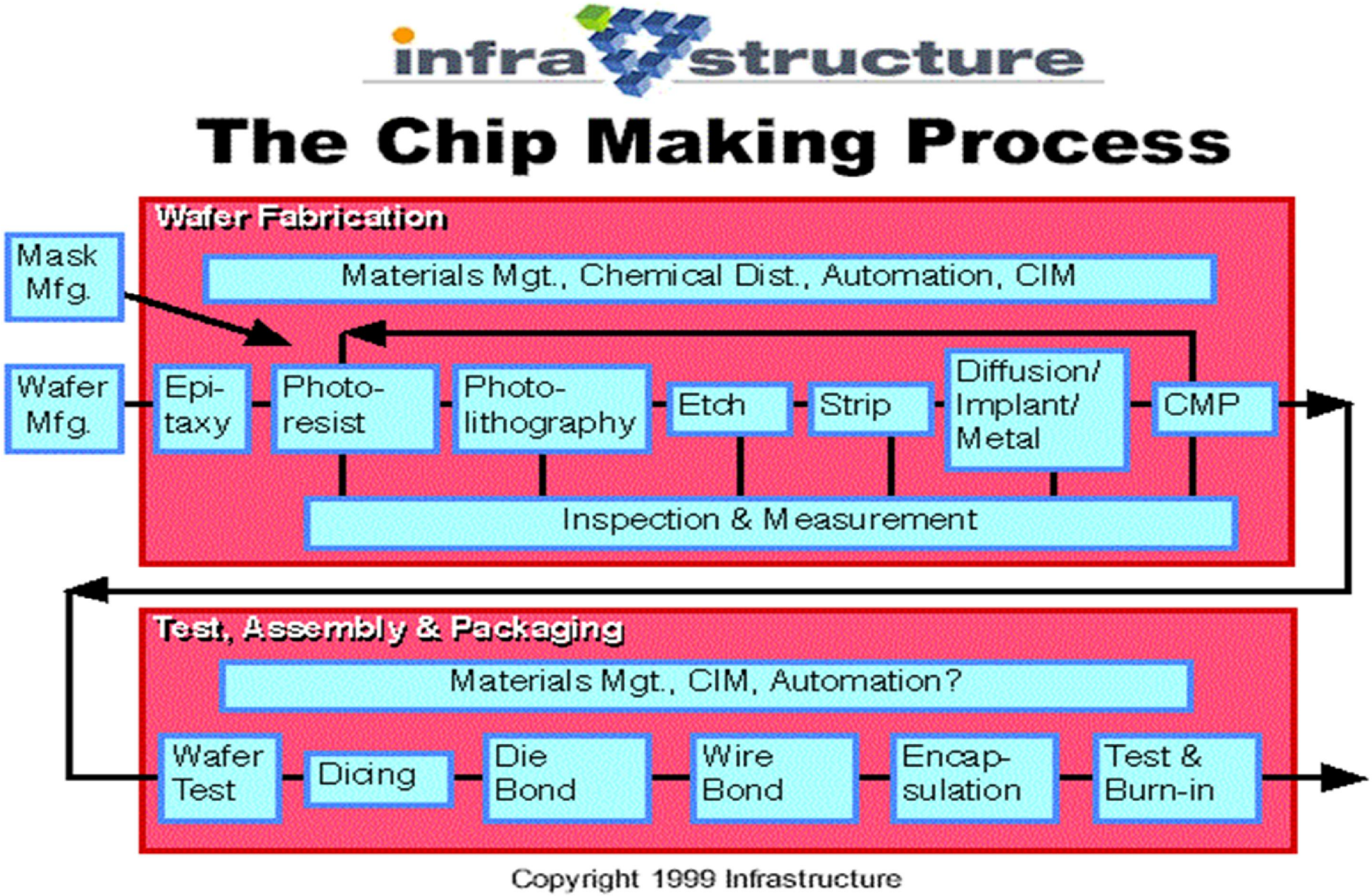
2.1.1 集成电路加工的基本操作

- 1、形成薄膜（二氧化硅、多晶硅、金属等薄层）
- 2、形成图形（器件和互连线）
- 3、掺　杂（调整器件特性）

木版年画

- 画稿
- 刻版
- 套色印刷

半导体芯片制作过程



硅片（wafer）的制作

infrastructure

Making the Wafer

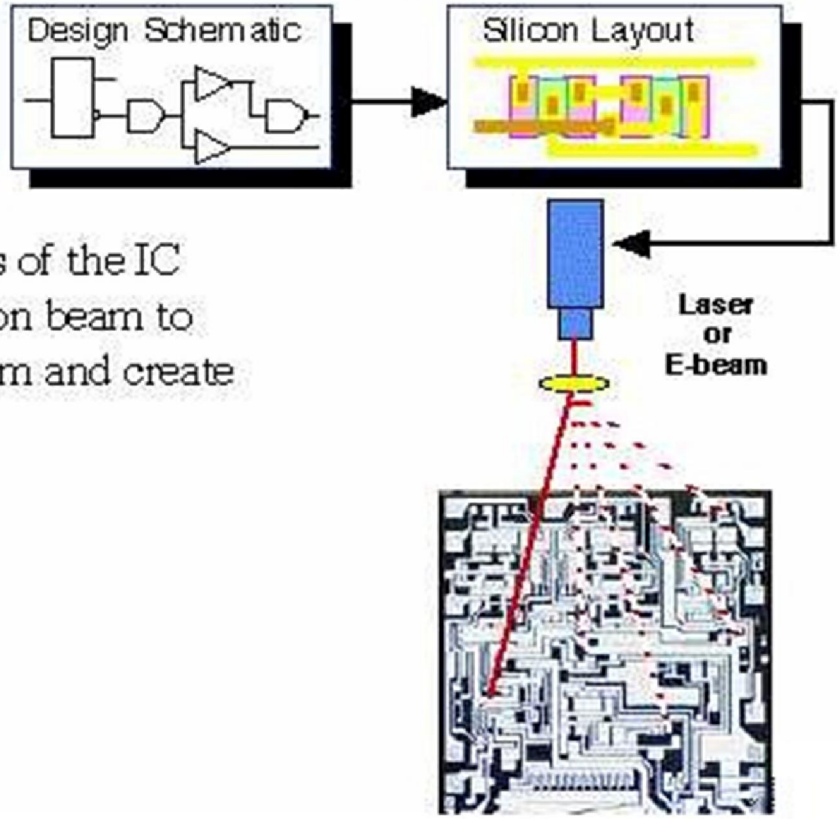
- The Process:
  - A seed crystal is suspended in a molten bath of silicon
  - It is slowly pulled up and grows into an ingot of silicon
  - The ingot is removed and ground down to diameter
  - The end is cut off, then thin silicon wafers are sawn off (sliced) and polished

掩模版（mask,reticle）的制作

infrastructure

The Mask Making Process

- The Process
  - Start with ultra-pure glass plates with a surface deposition of chromium.
  - Computer generated layouts of the IC drive a laser beam or electron beam to selectively remove chromium and create the mask or reticle.
- Design Driven:
  - increased complexity
  - long write times
  - New Product Acceleration

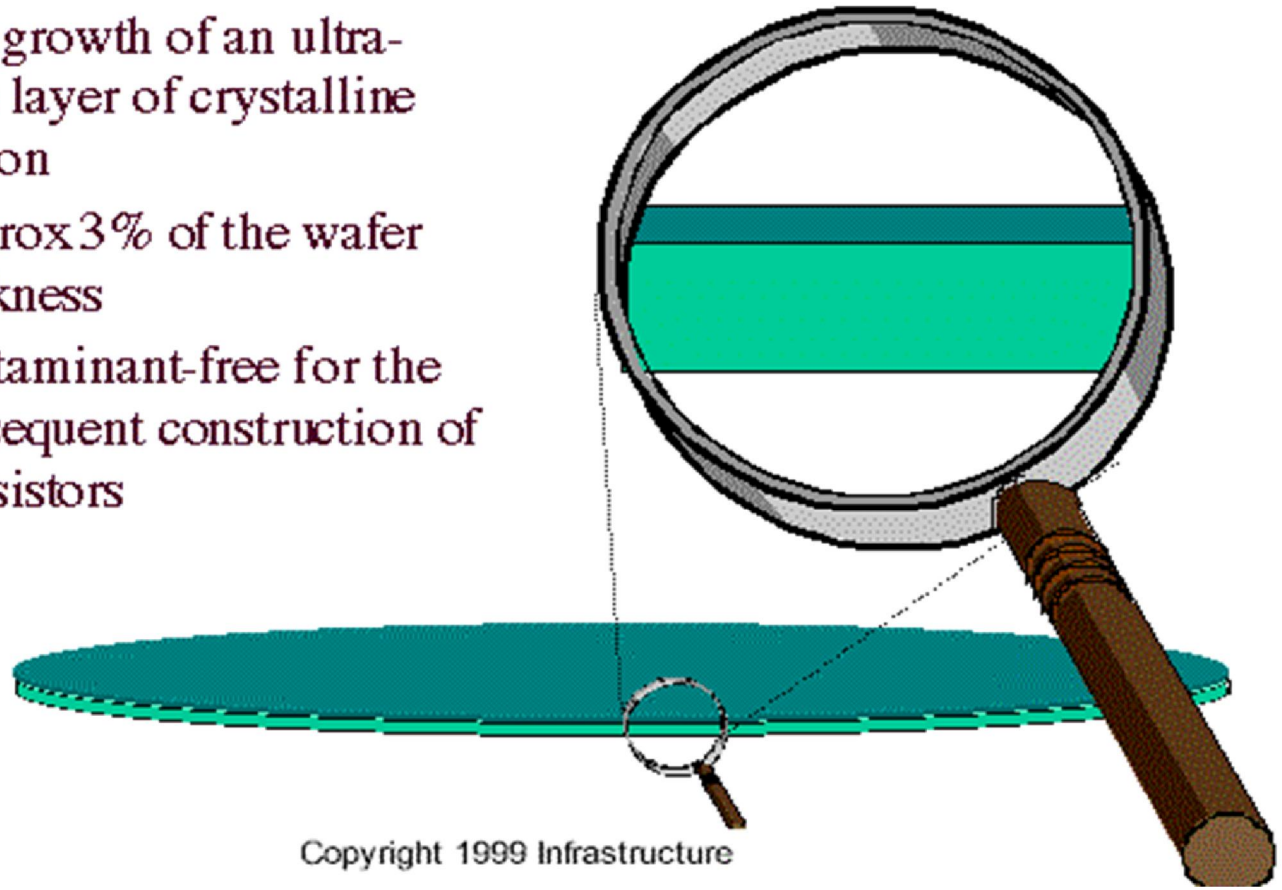


外延衬底的制作

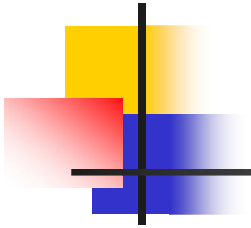
infrastructure

Epitaxy

- The growth of an ultra-pure layer of crystalline silicon
- Approx 3% of the wafer thickness
- Contaminant-free for the subsequent construction of transistors



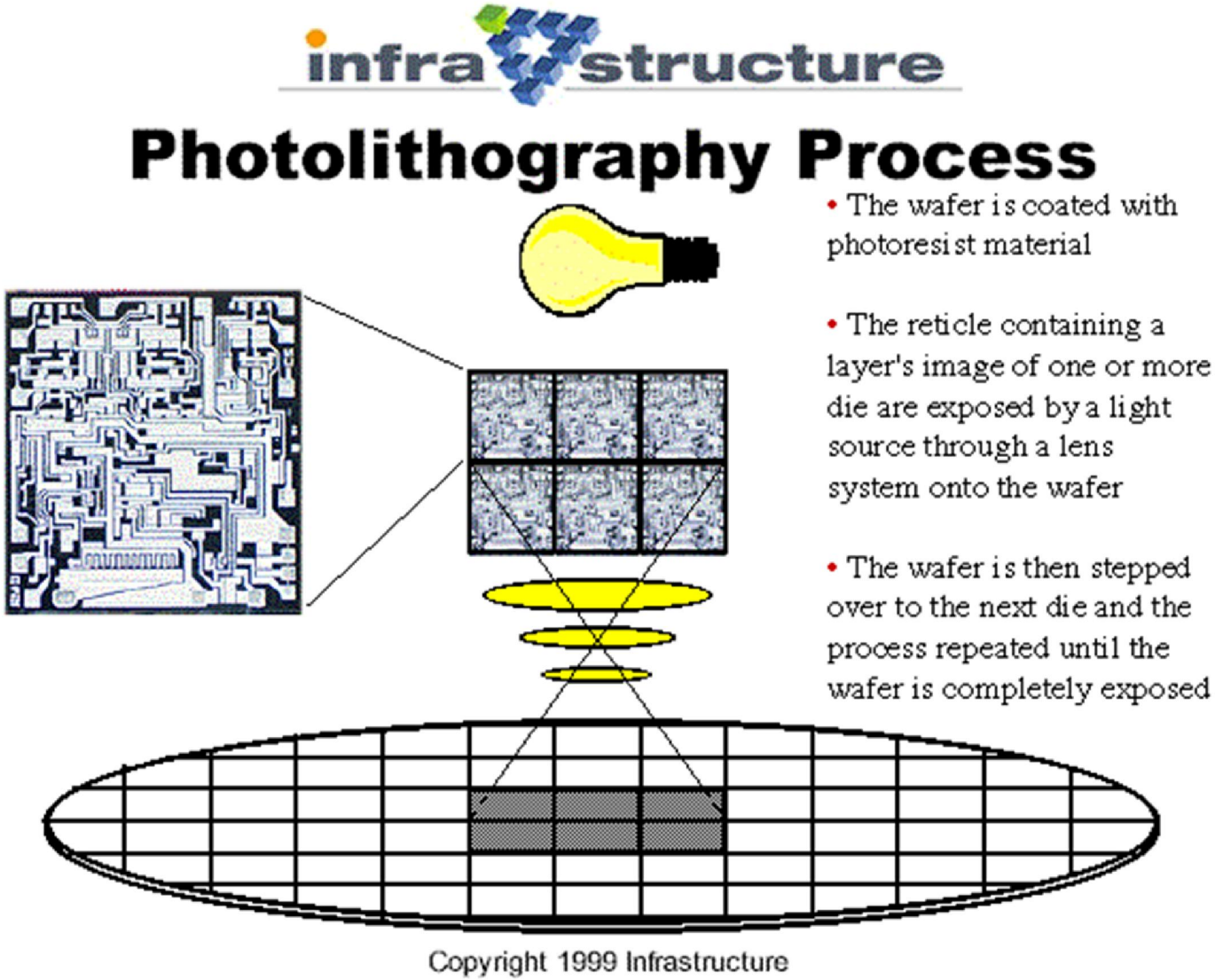
Copyright 1999 Infrastructure



1、形成图形

- 半导体加工过程：将设计者提供的集成电路版图图形复制到硅片上
- 光刻与刻蚀：半导体加工水平决定于光刻和刻蚀所形成的线条宽度

光刻（photolithography）

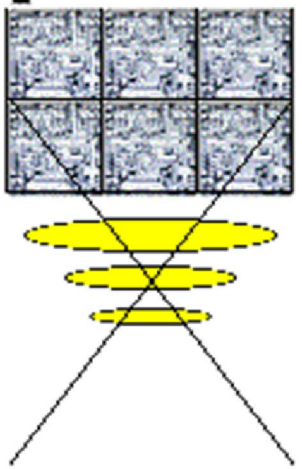


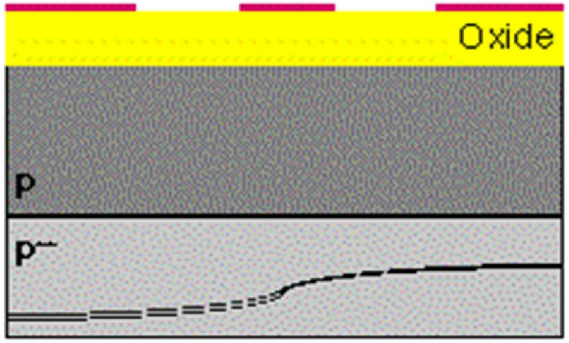
曝光（exposure）

infrastructure

Oxidation and Exposure

- The epi-wafer is exposed to high temperature to grow an oxide layer
- A layer of photoresist is spun onto the oxide
- The stepper exposes the pattern onto the photoresist
- The photoresist is then developed to leave the pattern on the wafer



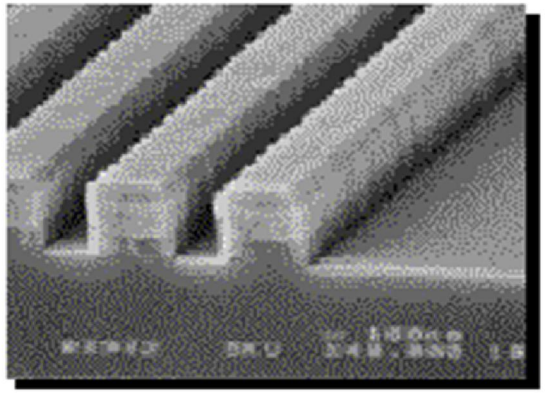


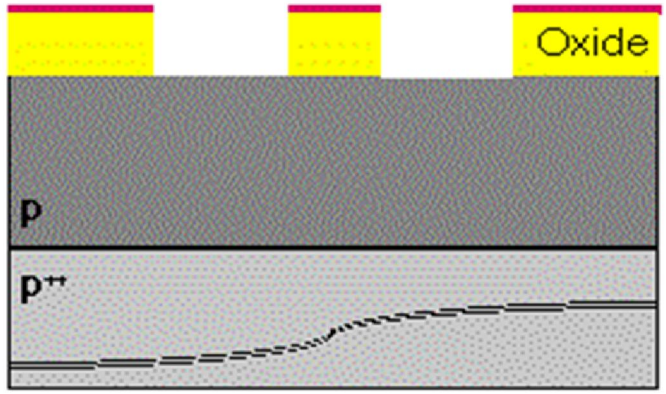
刻蚀（etch）

infrastructure

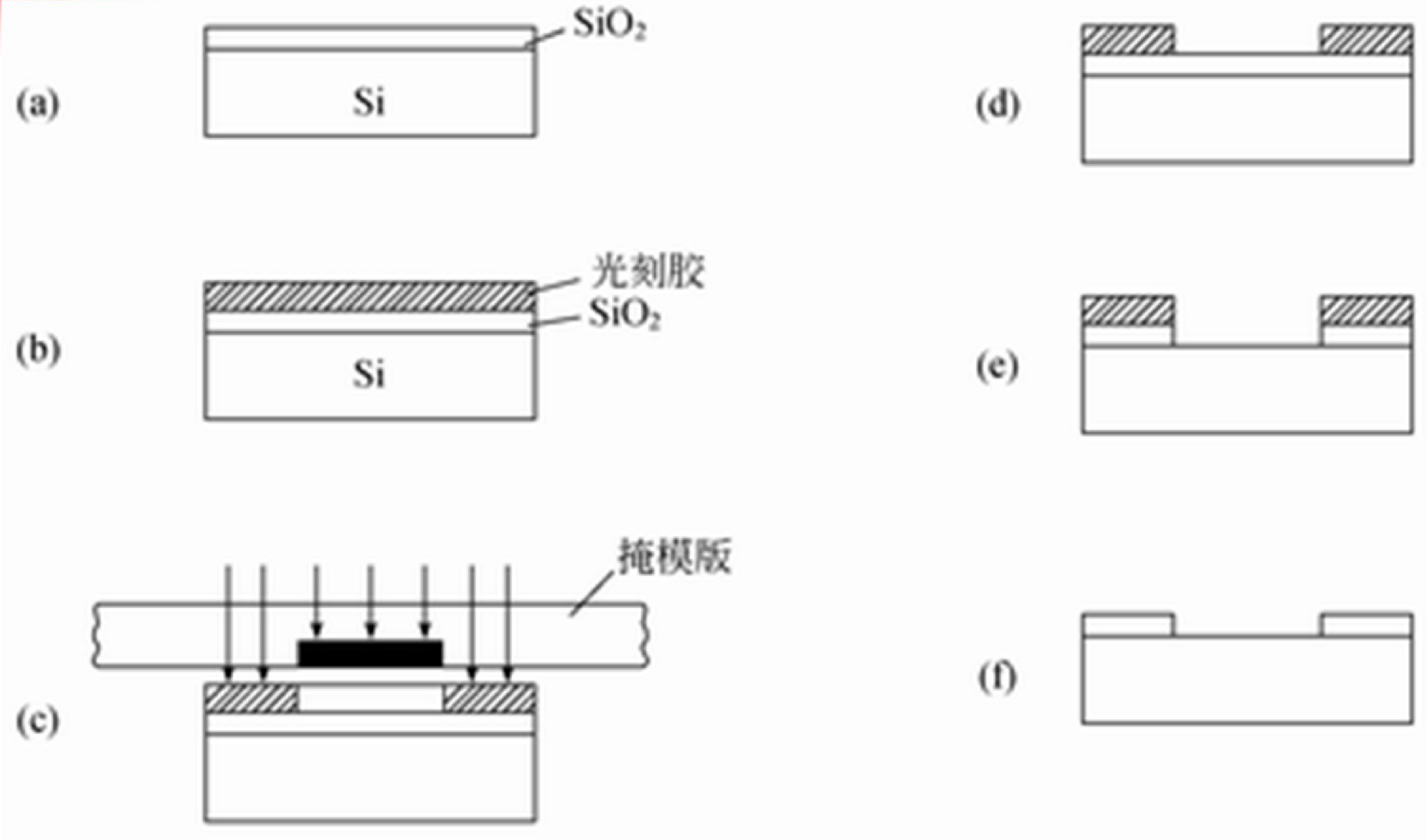
Etch and Strip

- An etch process (wet or dry) is used to remove the oxide where the photoresist pattern is absent
- The photoresist is then stripped completely off the wafer, leaving the oxide pattern on the wafer

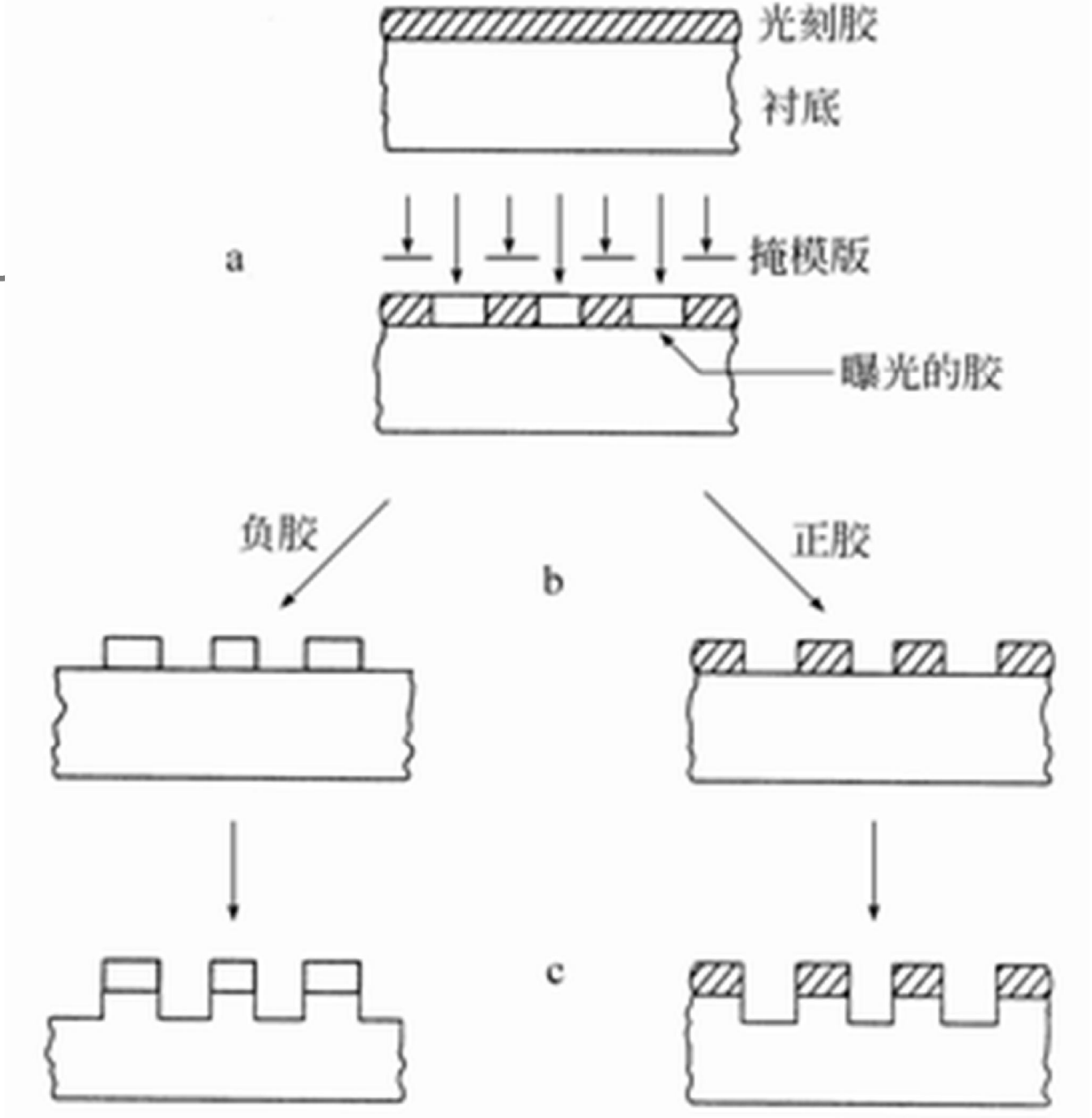




光刻的基本原理



正胶和负胶的差别

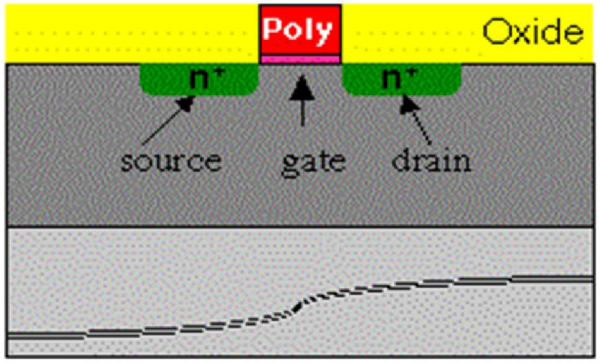


2、薄膜形成：淀积

infrastructure

Deposition

- Using the same oxidation & photolithography process, an opening is made in the oxide to build the transistor's gate region
- A thin gate oxide or silicon nitride is deposited via CVD or Chemical Vapor Deposition process to act as an insulator between the gate and the silicon
- This is followed by Physical Vapor Deposition (PVD) or "sputtering" of a conductive polysilicon layer to form the transistor's gate region

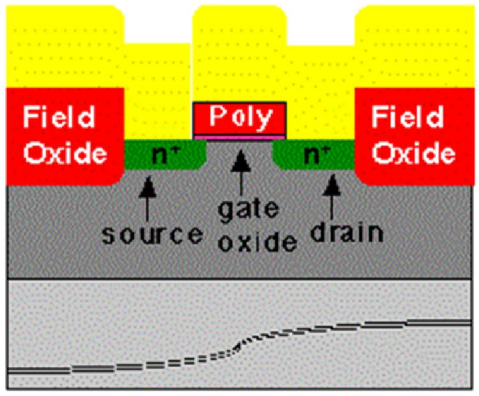


2、薄膜形成：氧化

infrastructure

Oxidation

- Various oxides are grown or deposited to insulate or protect the formed transistors
- Deep Field Oxides are grown to isolate each transistor from its adjacent partners
- Dielectric isolation oxides are deposited to insulate the transistors from the interconnecting layers which will be built above
- Passivation oxides are later deposited on top of completed wafers to protect the surface from damage

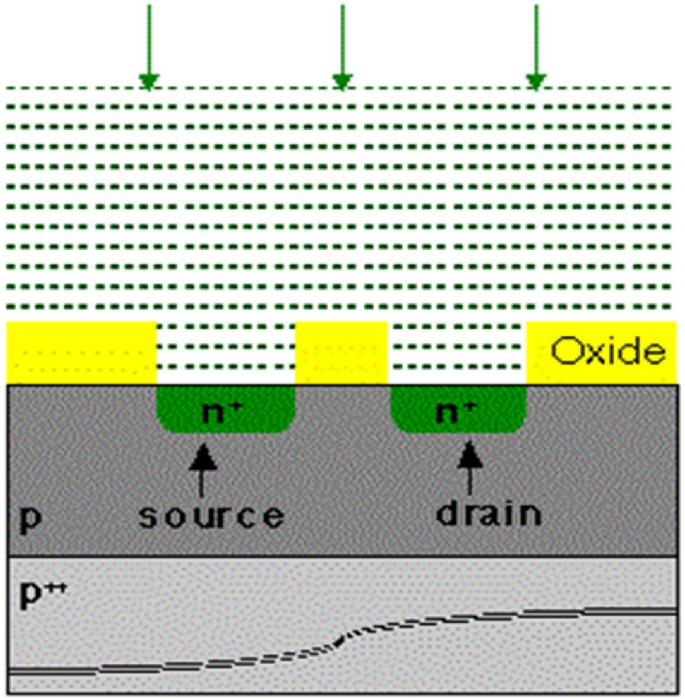


3、掺杂：扩散和注入

infrastructure

Diffusion and Implant

- The oxide acts as a barrier when dopant chemicals are deposited on the surface and diffused into the surface
- Alternatively, dopants may be bombarded into the silicon surface via an ion implant beam
- The induced ions create regions with different properties of the silicon semiconductor material
- These regions become the source and drain of the CMOS transistor

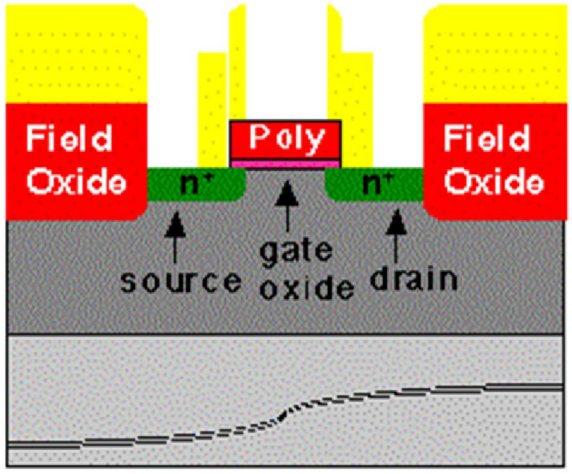


从器件到电路：通孔

infrastructure

Interconnect - Vias

- Using the same photolithography process, "via" contact holes are etched down to the three transistor regions which need to be connected to other components on the chip

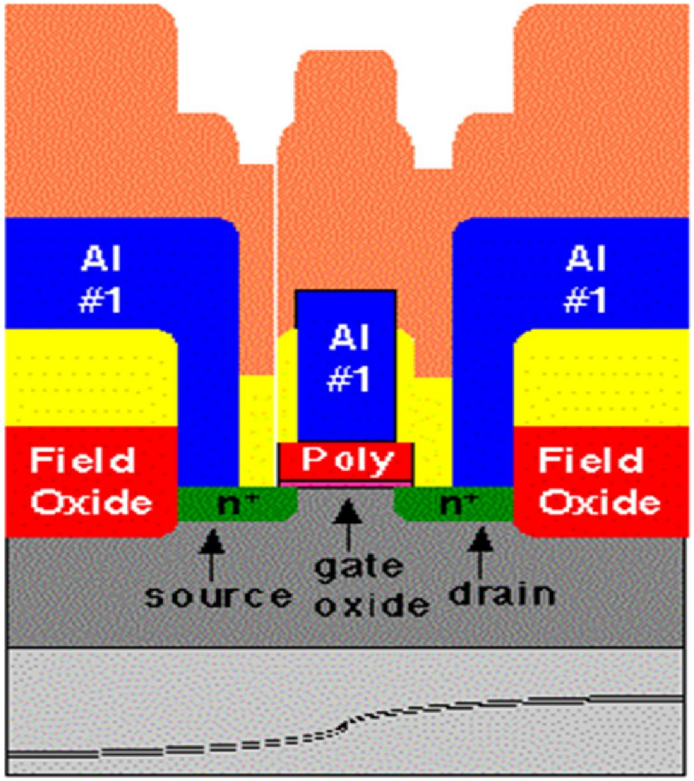


从器件到电路：互连线

infrastructure

Interconnect - Metalization

- A layer of aluminum is deposited on the surface and down into the via holes
- Excess aluminum is etched away after another photolithography process, leaving the desired interconnect pattern
- Another layer of dielectric isolation oxide is deposited to insulate the first layer of aluminum from the next one
- Note how the surface contours are developing with each process steps

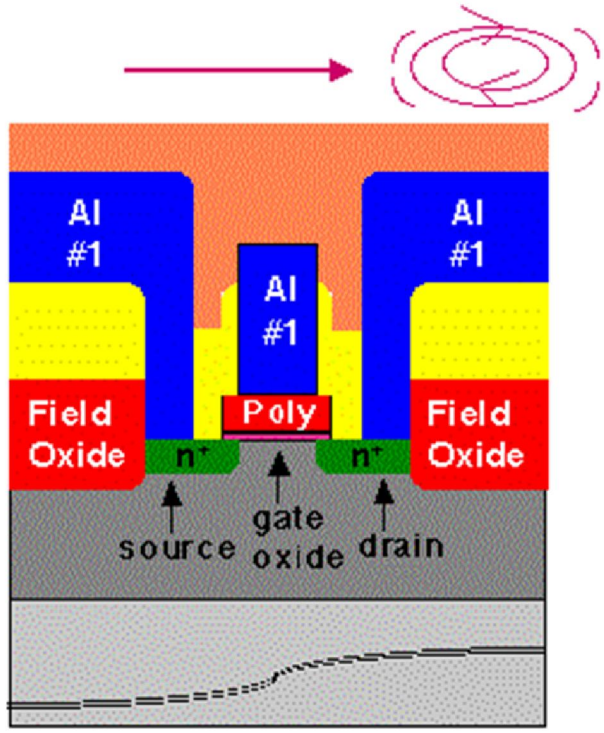


从器件到电路：多层互连

infrastructure

Chemical Mechanical Planarization

- CMP (Chemical Mechanical Planarization) is an abrasive process using chemical slurries and a circular (sanding) action to polish the surface of the wafer smooth
- The smooth surface is necessary to maintain photolithographic depth of focus for subsequent steps and also to ensure that aluminum interconnects are not deformed over contour steps

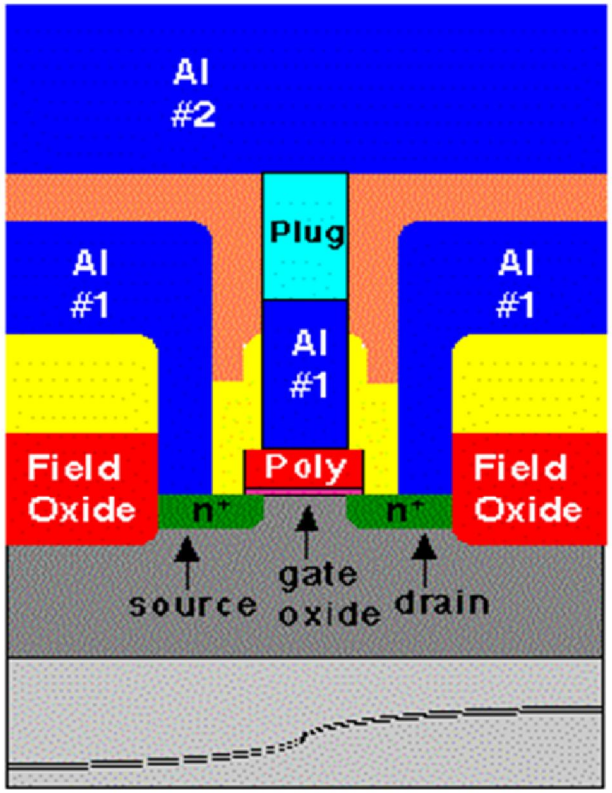


从器件到电路：多层互连

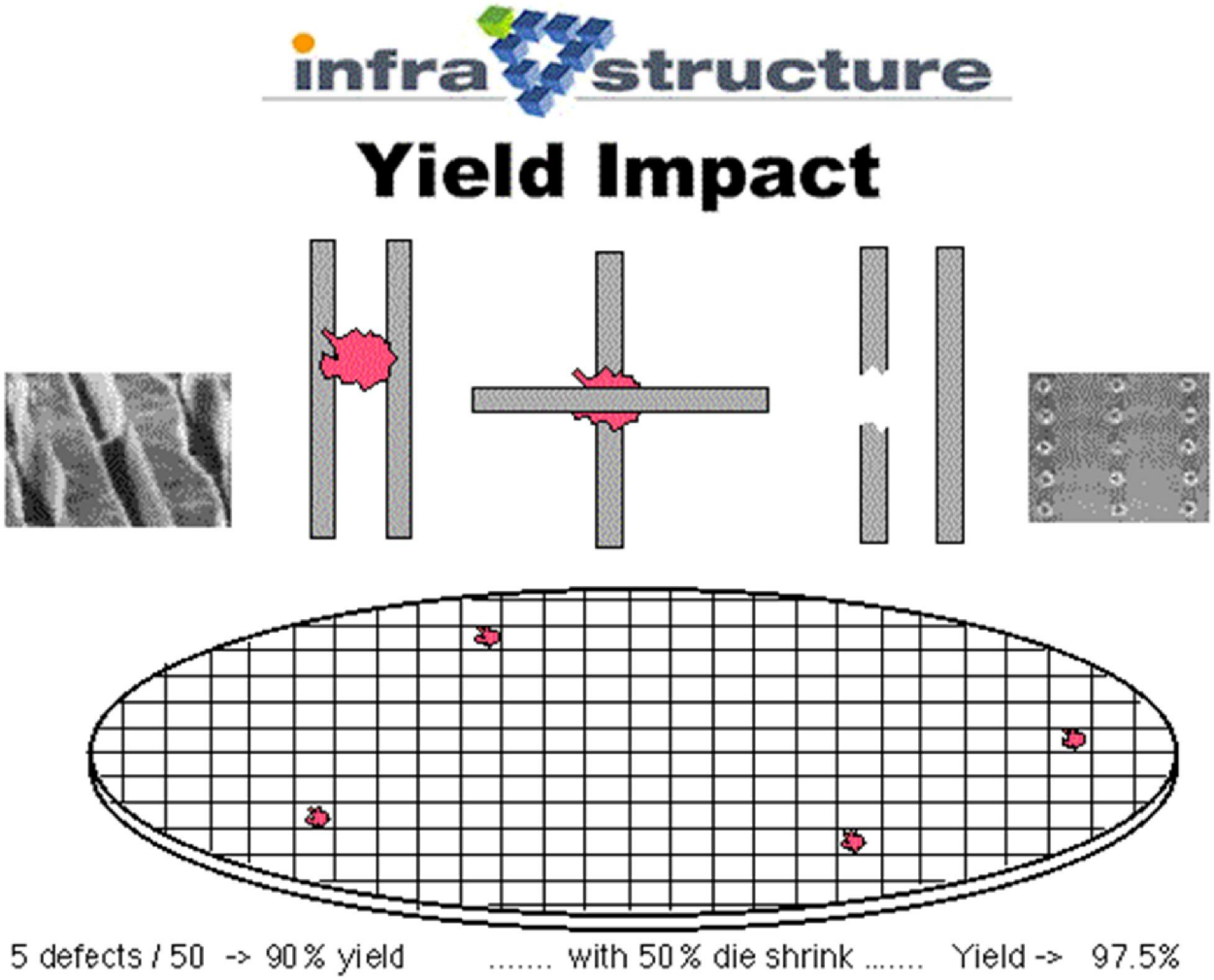
infrastructure

Interconnect - Layers

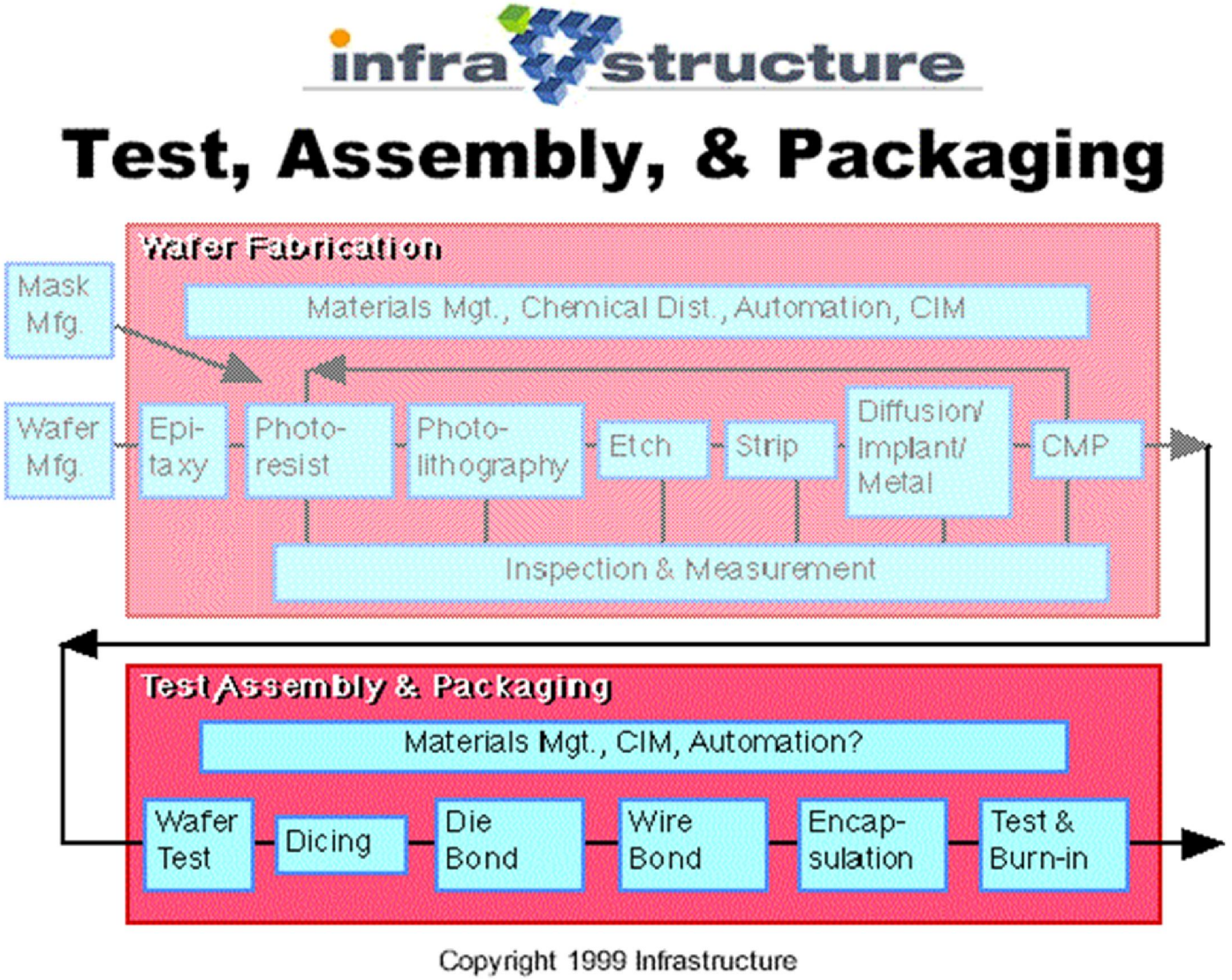
- Another set of via holes are etched in the dielectric isolation oxide to enable access down to the layer below
- Contact plugs are deposited (often tungsten) into the vias to reach down and make contact to the lower layer
- The next layer of aluminum is deposited, patterned and etched
- This process is repeated for as many interconnect layers as are required for the chip design



从硅片到芯片：加工后端



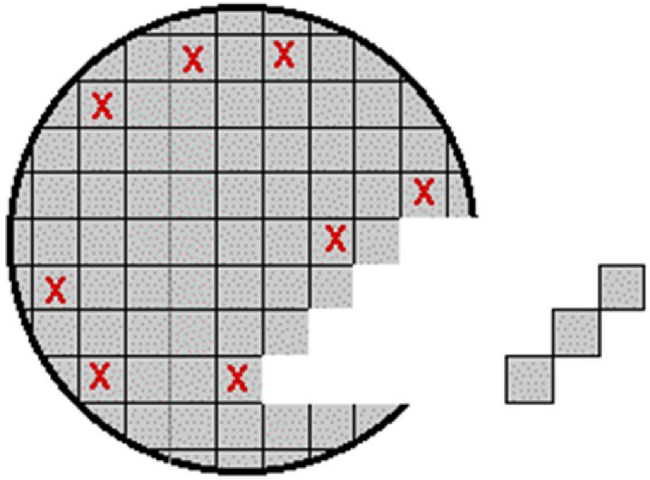
从硅片到芯片：加工后端

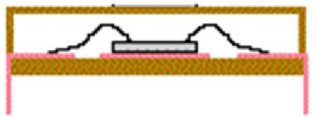


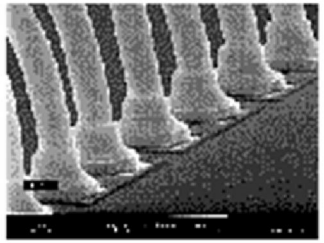
从硅片到芯片：加工后端

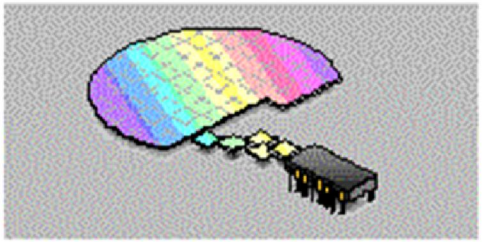
infrastructure

Assembly & Packaging









- Turning the wafer into a packaged chip