

实验内容、实验目的、时间安排

●实验内容:

- ●完成差分放大器的版图
- ●完成验证: DRC、LVS、后仿真

●目的:

•掌握模拟集成电路单元模块的版图设计方法

●时间安排:

●一次课完成差分放大器的版图与验证

实验步骤

- 1. 完成上节课设计放大器对应的版图
- 2. 对版图进行DRC、LVS检查
- 3. 创建后仿真电路
- 4. 后仿真(进度慢的同学可只选做部分分析)
 - DC分析: 直流功耗等
 - AC分析: 增益、GBW、PM
 - Tran分析:建立时间、瞬态功耗等

Display Option



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由Schematic创建Layout

- ●Schematic->Tools->Design Synthesis->Layout XL->弾出窗口 ->选择Create New->OK
- ●Virtuoso XL->Design->Gen From Source->弾出窗口
 - ●选择所有Pin
 - ●设置Pin的Layer
 - Update

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对管的共质心画法:相对位置放置

- ●设A管、B管为对管,共8个Multiplier
- ●将A管的前4个Multiplier合在一起,置于左上角
- ●将A管的后4个Multiplier合在一起,置于右下角
- ●将B管的前4个Multiplier合在一起,置于右上角
- ●将B管的后4个Multiplier合在一起,置于左下角



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对管的共质心画法: 层间互连单元的调用

●调用单元

●快捷键 o

●设置

- ●Column: Contact列数
- ●Row: Contact行数
- ●其余可供调用的层间互连单元
 - •M1_NWELL
 - •M1_PSUB
 - •M2_M1
 - •M3_M2
 - •M4_M3





Create Contact

M1_POLY2

centerCenter

Cancel

Hide

Auto Contact

Contact Type

Justification

Help

对管的共质心画法:连线

●A管中前4个Multiplier的连线

- ●挪动B管前4个Multiplier的位置, 复制上图中的相关连线(注意:使 用上下镜像功能)
 - ●按c,鼠标左键拉框,选定一组连线
 - ●按F3,选择上下镜像
 - ●将复制后的连线放到合适的位置



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对管的共质心画法:连线、隔离

- ●使用M1_PSUB将N型MOSFET围起来
 - ●固定衬底电压、隔离数字干扰



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完成放大器的版图

●例子, 仅供参考。



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显示未完成的连线: 查找未完成的连线时使用



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模拟单元电路设计

查找DRC错误标识

- ●Verify->Markers->Find, 弾出窗口
- ●设置Zoom To Markers
- ●按Apply显示当前DRC错误标识,按Next显示下一个标识
- ●回到版图窗口,按Shift+z缩小显示目标,查看标识的具体原因

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查找LVS的未匹配处

- 首先: LVS结束后, 查看Output结果
- 若查看结果很难找出未匹配处,请按如下方法查找
 - 1. 打开电路的extracted view
 - 2. 在extracted view中:Verify->LVS->Error Display, 弹出窗口
 - 3. 设置Auto-Zoom,按First、Next可显示LVS失配(佐以shift+z)
 - 4. 记录失配原因与坐标,回到Layout View查看该坐标处的版图信息



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后仿真(第一步): Build Analog



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后仿真(第二步): Create Symbol

- 1. 打开任意一个Schematic View
- 2. Design->Create Cellview->From Cellview, 弹出右上窗口
- 3. 点击Browse,弹出右下窗口
- 4. 选后仿单元的Analog_extracted

参考由Schematic生成Symbol

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后仿真(第三步):仿真设置

- 1. 调用analog_extracted生成的symbol,创建仿真电路
- 2. 启动ADE (Analog Design Environment)
- 3. ADE->Setup-> Environment, 弹出窗口
- 4. 在Switch View List中添加analog_extracted

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